Manufacturing efficiency improvement through MBE recipe optimization

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Abstract

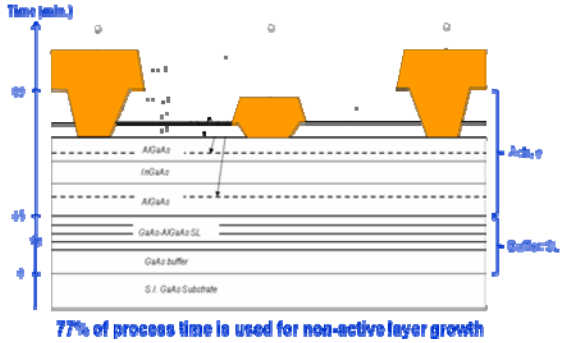
During the MBE growth process of a pHEMT structure, the buffer layer and superlattice generally take more than 50% of the overall resources and time. This paper focuses on the reduction of the MBE growth time by optimizing the buffer and superlattice structures, discusses the challenges associated with thinning these layers, and reports results of overall manufacturing efficiency improvement at Skyworks.

Introduction

Since the initial development of AlGaAs/InGaAs based pHEMT device 30 years ago, there were numerous publications on refining or optimizing the device structure, but all focused on active device layers to improve device's electrical performance. To the best of our knowledge, there are few literature reports discussing optimization of buffer layer and superlattice structure to improve manufacturing efficiency of MBE grown epi wafers. This paper reports the progress of a manufacturing efficiency improvement project at Skyworks, discusses the key aspects that need be considered when reducing the buffer and superlattice thickness, and reports over 30% throughput improvement through MBE growth recipe optimization.

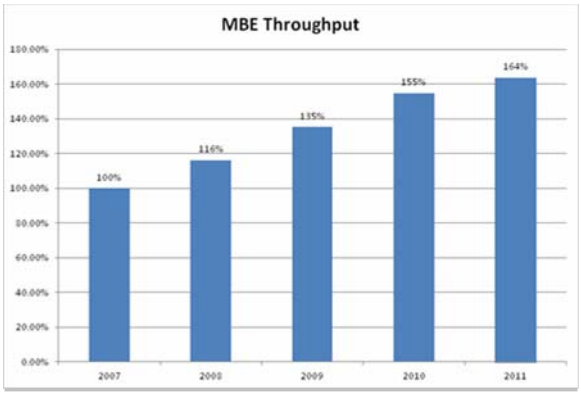
Results and discussion

A typical pHEMT structure used for today's switch applications consists active device layers, such as n-GaAs layers, AlGaAs Schottky layer, and InGaAs channel layer, and GaAs buffer layer and superlattice (Fig.1).



To grow a high quality pHEMT epi structure, one has to start with a clean crystal surface, which is achieved by thermal desorption of native oxide on substrate surface. Since thermal desorption of native oxide process tends to roughen the surface of GaAs substrates, the growth of a buffer layer is necessary to provide a clean and smooth starting surface for consecutive growth of active device layers. On the other hand, while the thermal desorption process generally removes most of the surface contamination with the native oxide, it often levees some residual contaminations, such as carbon, silicon, and oxygen. Because of those residue surface contaminations, a

buffer layer is also important to keep them away from the active device layers. In addition to a GaAs buffer, a GaAs/AlGaAs superlattice in pHEMT structure is mainly used for blocking hot electrons injection from InGaAs channel into buffer to minimize leakage current through the buffer layer. Combining with GaAs buffer, the supperlattice also act as a spacer to separate the channel and the contamination at substrate/buffer interface. During MBE growth cycle of a typical pHEMT structure, only less than 30% of the time is spent to grow the active device layers. The majority of the time is used for native oxide desorption process, the buffer layer, and the supperlattice growth. While those process steps are essential to obtain high quality pHEMT devices with good electrical performance, it is desirable to minimize these process steps as much as possible in order to maximize production efficiency or throughput, which will ultimately translate into per wafer cost reduction. The goal for this project is to improve MBE throughput by 30%. We took evolutionary approach by dividing the whole process into several phases in order to minimize production risks. The first step in this recipe optimization process is to select the right parameters that are sensitive to thinner buffer, short period of superlattice, and short thermal desorption to ensure there is no sacrifice of any device performance. Among the typical material and device parameters, we paid particular attention to surface roughness, pinch-off voltage, leakage current, and breakdown voltage. We found that the minimum thickness of buffer layer and supperlattice is not limited by the surface roughness and cleanness, but rather by “back gating” effect from residual carbon at substrate/buffer interface. The higher the carbon concentration, the thicker the buffer and superlattice needed to eliminate the “back gating” effect. By modifying the native oxide desorption process, we have successfully minimized carbon contamination at substrate surface, which allowed us to reduce the overall thickness of buffer and superlattice, therefore shorten the growth recipes. Over 30% improvement of MBE production throughput has been achieved by optimizing the growth recipe. PHEMT devices processed based on the epi structure with 30% reduction of recipe time were fully characterized through all the metrologies and device parametric, including high temperature operating life (HTOL) test. The devices performance data showed no sign of degradation due to shortening MBE growth time. The modified process has been implemented to most high running products through different phases. The year-over-year MBE throughput improvement through recipe optimization and other projects at Skyworks is shown in Fig.2.



Year over year MBE throughput improvement at Skyworks through recipe optimization and other engineering projects.