TCAD Assessment of Gate-Geometric Nano-scale In$_{0.52}$Al$_{0.48}$As-In$_{0.53}$Ga$_{0.47}$As Double-Gate HEMT for High Breakdown Voltage

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InP-based Heterojunction transistors exhibits outstanding RF performances having cut-off frequency ($f_T$) of 644 GHz. In spite of higher input costs of InP based HEMTs, their lower noise figures, better thermal conductivity, high electron density (due to higher conduction band offset, $\Delta E_c=0.52$ eV) and high mobility that exceeds 10000 cm$^2$/Vsec, find reliable applications in low-noise amplifiers (LNA) designs. For further enhancing RF performance, the basic thumb rule of gate-length ($L_g$) scaling is followed in FETs. However reducing the gate length below 100 nm leads to onset of short channel effects (SCEs) in the devices. Double-gate high electron mobility transistor (DGHEMT) has step-up a new paradigm to reduce short-channel effects (SCEs) in the field of compound semiconductor devices.

However, with all the advantages DGHEMT still employs InGaAs channel thus making it susceptible to all the intrinsic drawbacks of this material viz. lower energy band gap (0.52 eV) and higher impact ionization coefficient ($\alpha$). Thus narrow band gap of InGaAs limits the power applications of these devices. As high breakdown voltage is one of the necessary requirements for achieving superior power performance, various approaches have been adopted to overcome this intrinsic shortcoming of InGaAs channel devices, some of these include channel engineering etc. Another approach to suppress impact ionization is Field-Plate technology, field plates with wide recess are an attractive approach as they do not involve the epitaxial modification in the device structures.

This field-plate technology becomes more attractive with the scaling of gate-length as the limitation in lithography for submicrometer gate formation involuntarily leads to the formation of various gate geometries like T-Gate, $\Gamma$-Gate, Camel-Gate and many more. The formation of these geometries is attributed to careful attention given to the technological details of gate formation, layer design and growth by multilevel resist process using e-beam lithography and reflow treatment. These geometries are also unavoidable because with the gate-length scaling the parasitic gate resistance ($R_g$) increases proportionally to $1/L_g$, thus deteriorating power gain and noise figures. Therefore, with scaling, $R_g$ must be kept as low as possible. These gate-geometries are a good compromise between these two, as shorter $L_g$ (corresponding to the base) and low value of $R_g$ (corresponding to the wide area at the top head) leads to good device performance. With slight modifications, these gate geometries can also be used to reduce electric field under the gate at the drain side particularly in the case of $\Gamma$-Gate/$T$-Gate geometry. Further by Field-Plate technology (or Gate-Engineered Technology) the device can be customized as per the requirements by just modifying the final steps in the fabrication process.

Though previous works have explored the Gate-Engineered HEMT for improved breakdown characteristics, while in the present work the effects of Gate Engineering on Recessed DGHEMT have been studied, considering the importance of breakdown in InGaAs channel based HEMTs.

This work is carried out using Blaze module of Silvaco Atlas Device Simulator for III-V, II-VI, IV-IV, etc. materials and devices with positional dependent band structures (heterostructure). It accounts for the band discontinuity at the heterojunction by modification to the charge transport equations. Basic equations to be solved are the Poisson’s equation, continuity equations for electrons and holes, and transport equations.

Fig.1 gives the schematic view of the simulated structure of the DGHEMT device while Fig. 2 shows the different gate-geometries studied. Fig. 3 plots the electric field profile at the gate interface, as the peak electric field at the gate edges is responsible for off-state breakdown. $\Gamma$-Gate/$\Gamma$-Gate are more suitable from breakdown point of view, as they effectively reduces the peak electric field on the drain side both in the channel and at gate interface. On the other hand, Fig. 4 plots $f_{\text{max}}$ variations with gate-voltage of different gate-geometric DGHEMTs. As compared to $f_T$, $f_{\text{max}}$ have far more complex dependency on large number of intrinsic ($g_{\text{ds}}$, SCEs, etc.) and extrinsic (access resistances (gate and source) and parasitic capacitances) parameters including $f_T$. As the wide upper area of gate-geometries results in lower gate resistances therefore the variation of gate resistance with different gate-geometries is also considered.
As can be seen from the figure, T-Gate shows maximum while N-Gate minimum values of \( f_{\text{max}} \). This is attributed to the lowest gate resistance value of T-Gate by the virtue of its wide upper area. From the above discussion on various gate-geometries, \( \Gamma \)-Gate and T-Gate devices perform better as compared to N-Gate and IL-Gate devices in reducing the peak electric field values and enhancing the breakdown voltage in the device. As T-Gate leads to additional parasitic resistance/capacitance on the source side, therefore \( \Gamma \)-Gate device appears to be more suitable candidate as far as \( f_T \) performance of the device is concerned. However, T-Gate device have the maximum \( f_{\text{max}} \) values. Therefore, \( \Gamma \)-Gate appears to be the most suitable candidate to enhance the overall performance as it not only effectively reduces the peak electric field at the drain edge of the gate but also shows lesser degradation in RF characteristics. So, depending upon the device applications, Gate-Geometries can be modified to improve device performances. For eg., peak electric field in the channel should be the focus when device operates in saturation mode as in LNAs, whereas for power application peak field at the gate should be optimized as the device works in class B mode for better efficiency.