Impact of step edges on trapping behavior in N-polar GaN HEMTs

Nicole Killat[1,*], Michael J. Uren[1], Seshadri Kolluri[2], Stacia Keller[2], Umesh K. Mishra[2], and Martin Kuball[1]

[1]Center for Device Thermography and Reliability (CDTR), H.H. Wills Physics Laboratory, University of Bristol, Tyndall Avenue, Bristol BS8 1TL, United Kingdom
[*]E-Mail: Nicole.Killat@bristol.ac.uk, Phone: +44 117 9288750

[2] Department of Electrical and Computer Engineering, University of Santa Barbara California, Santa Barbara, CA 93106, USA

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ABSTRACT

Electroluminescence imaging in combination with DC and pulsed IV characterization was used to study the impact of step edges on the performance of N-polar AlGaN/GaN HEMTs grown on vicinal substrates. The presented methodology demonstrates the interaction of the two-dimensional electron gas with the step potential profile induced by the presence of step edges. Pulsed IV characteristics reveal that step edges have an effect on the behavior of surface traps, potentially affecting device reliability.

INTRODUCTION

With regard to novel device structures, growth on vicinal substrates has been used to achieve high-quality N-polarity GaN devices [1]. However, this step-growth process leads to the formation of terraces separated by oriented multi-atomic steps on the GaN-based epilayers. This was reported to result in an anisotropy of charge carrier mobility and sheet resistance [2, 3]. Nath *et al.* suggested an electrostatic model, which considers the steps forming a potential profile, leading to a lateral confinement of the two-dimensional electron gas (2DEG) [4]. The impact of these effects on the device performance can be crucial and needs to be considered for GaN device reliability and fabrication. Moreover, growth on off-cut SiC substrates is often used for the more common Ga-polarity devices; hence, understanding the role of step edges is of generic importance. This work studies the impact of vicinal substrate growth on the properties of N-polarity AlGaN/GaN HEMTs using electroluminescence imaging in combination with electrical characterization.

EXPERIMENTAL DETAILS

Measurements were performed on AlGaN/GaN HEMTs grown by MOCVD on a sapphire substrate with a miscut of 4°. The layer structure consisted of a 1.5-µm-thick GaN buffer, followed by a 30 nm AlGaN layer, a 25-nm-thin GaN epilayer, a 2-nm-thin AlGaN layer and 5 nm silicon nitride passivation. More details on the growth of the structure studied can be found in Ref. [2]. Two different orientations of the gate contact with respect to the multi-atomic steps, caused by the miscut, were studied: Device A with conduction parallel to the steps and device B with conduction perpendicular to the steps. The DC and pulsed IV characteristics were investigated on several devices using a Keithley 4200-SCS and a Dynamic IV Analyzer (DIVA). For the pulsed IV measurements, a 1 µs pulse was applied from quiescent biases of either V_{GSq}= V_{DSq}= 0 V or V_{GSq}= -5 V, V_{DSq}= 20 V. The electrical data was compared with the electroluminescence (EL) data obtained in on-state. To avoid EL absorption from contacts, EL images were acquired from the bottom of the device using a retro-reflector setup, enabling optically probing of the whole device area, between and underneath the metal contacts.

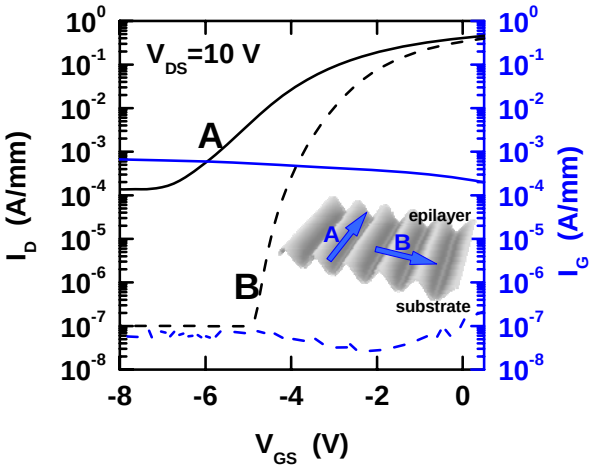

FIGURE 1. TRANSFER CHARACTERISTICS IN THE SATURATION REGIME FOR DEVICE A (SOLID LINE) AND DEVICE B (DASHED LINE) WITH L_G= 0.9 µM, L_{S-D}= 3.3 µM AND W= 150 µM. THE INSET ILLUSTRATES THE DIRECTION OF THE CURRENT WITH RESPECT TO THE POTENTIAL PROFILE INDUCED BY STEP EDGES.

RESULTS AND DISCUSSION

Fig. 1 shows typical transfer characteristics for device A and B for V_{DS}= 10 V. Device A with conduction parallel to the steps exhibits a larger drain current, which can be attributed to an anisotropy in mobility reported previously in Ref. [2, 3]. This effect results in a lower sheet resistance for conduction parallel to the multi-atomic steps, in contrast to conduction perpendicular to the step edges in device B with its higher sheet resistance. Most interestingly, there is a lower slope in the vicinity of the pinch-off voltage for device A when compared to device B, i.e., a less sharp pinch-off. This confirms that step edges will induce a potential modulation (inset of Fig. 1) and there is a wide distribution in pinch-off voltages for this case, whereas only a single pinch-off voltage will be present for device B. This is in agreement with the electrostatic model of Nath *et al.* suggesting a lateral quasi-one-dimensional potential profile across the steps, which results in a local confinement of the 2DEG [4].

Fig. 2 shows an EL image and profile for both device orientations. The EL profile appears broader in the case of device A when compared to the rather sharp EL peak for device B. This broadening

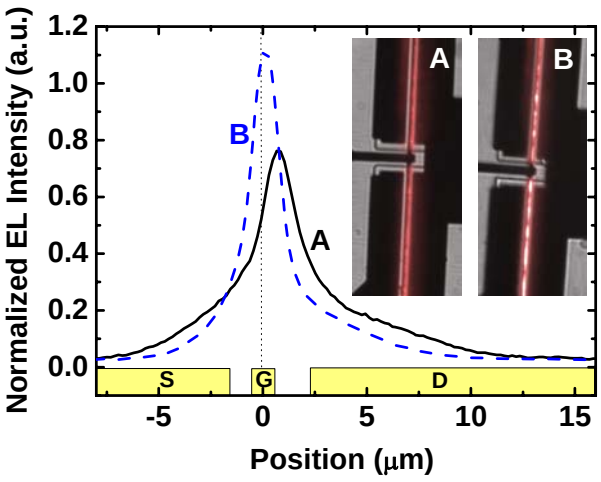

FIGURE 2. ELECTROLUMINESCENCE (EL) PROFILE IN THE SOURCE-DRAIN GAP FOR DEVICE A (SOLID LINE) AND DEVICE B (DASHED LINE), OPERATED AT V_{GS}= 0 V AND V_{DS}= 20 V, MEASURED THROUGH THE BACK OF THE DEVICES, I.E., THROUGH THE SUBSTRATE, TO ENABLE PROBING BOTH BETWEEN AND UNDERNEATH CONTACTS. THE EL INTENSITY WAS NORMALIZED BY THE DRAIN CURRENT. THE INSET SHOWS THE EL IMAGE OVERLAID WITH THE WHITE LIGHT IMAGE OF THE DEVICE.

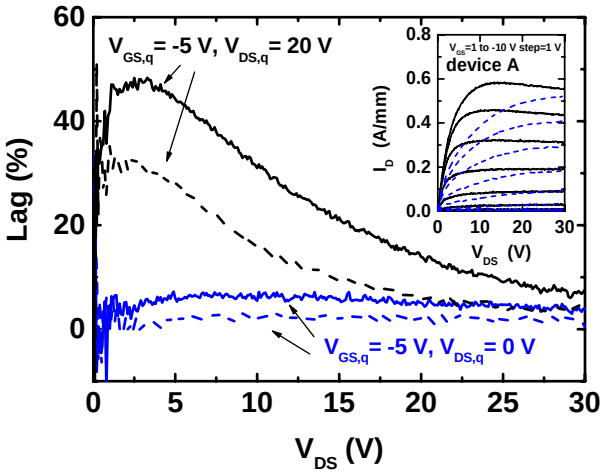

FIGURE 3. PULSED IV CHARACTERISTICS FOR DEVICE A (SOLID LINE) AND DEVICE B (DASHED LINE). THE RATIO BETWEEN THE PULSED IV CHARACTERISTICS AT THE CLASS-B QUIESCENT BIAS POINT OF V_{GSQ}= -5 V, V_{DSQ}= 20 V (OR V_{GSQ}= -5 V, V_{DSQ}= 0 V) AND V_{GSQ}= V_{DSQ}= 0 V IS SHOWN, ALL COMPARED AT V_{GS}= 0 V. INSET SHOWS THE ORIGINAL PULSED IV CHARACTERISTICS FOR DEVICE A, WITH THE QUIESCENT BIAS POINT OF V_{GSQ}= V_{DSQ}= 0 V (SOLID LINE) AND V_{GSQ}= -5 V, V_{DSq}= 20 V (DASHED LINE). THE PULSE DURATION WAS 1 μS WITH A REST TIME BETWEEN PULSES OF 1 MS.

of the EL profile is a consequence of the electric field being more spread out in the source-drain gap, which can be attributed to surface traps in the access region of the device leading to a ballasting effect. Furthermore, a homogenous EL emission along the gate width was observed for device A (inset of Fig. 2). In contrast, device B demonstrated a very inhomogeneous EL distribution along the gate. The more uneven electric field distribution in device B is related to an increased sensitivity to any field fluctuations consistent with reduced surface trapping and increased peak electric field.

Support for this interpretation can be gained from pulsed IV measurements. Typical lag measurements for both device orientations are presented in Fig. 3 for different quiescent bias points. Measurements at V_{GSq}= -5 V and V_{DSq} = 0 V show almost no lag denoting no trapping on the source side of the gate. The inset illustrates the pulsed IV characteristics for device A for the quiescent bias point V_{DSq}= 20 V, V_{GSq}= -5 V and for V_{DSq}= V_{GSq}= 0 V. Device A exhibits a strong knee-walkout under the influence of the high drain field, leading to a higher lag when compared to device B. A higher lag relates to a stronger contribution from surface traps in the case of conduction parallel to the steps, suggesting that the resulting potential profile enhances not only the conduction in the channel, but also the hopping conduction at the surface [5]. In consequence, the virtual gate spreads out further into the gate-drain gap, leading to a broader electric field distribution, as observed in the EL profile if conduction along step edges takes place. This is also consistent with a lower lag for device B, as any potential barrier induced by the step edges will reduce hopping through trap states and consequently the impact of surface traps on the conduction in the channel. The result is a more confined electric field at the drain edge of the gate contact. This effect could have a significant impact on device reliability and is likely to occur in any off-cut grown device structure.

CONCLUSION

The electrical and EL behavior of N-polarity AlGaN/GaN HEMTs grown on vicinal substrates was studied with regard to different orientations of the current with respect to the step edges. Devices with conduction parallel to the steps exhibited higher drain currents, but worse pinch-off behavior, which agrees with the electrostatic model of a step potential profile induced by step edges. The inhomogeneous EL profile along the gate demonstrated the strong interaction of the 2DEG with the potential profile. Pulsed IV characteristics revealed that the step edges also have an impact on the behavior of surface traps, which are crucial for device efficiency, reliability and power performance.

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ACRONYMS

HEMT: High Electron Mobility Transistor
2DEG: two-dimensional electron gas