A Call to Higher Quality in GaAs

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Abstract

This extended abstract describes the methodology that was followed and the results of an initiative to increase GaAs product quality. The methodology was divided into 4 main sections: NPI phase gate methodology, NPI product qualification, product safe launch, and product sustainability. The success of the initiative was measured over a period of 26 months by quantifying the reduction in customer quality incidents.

BACKGROUND

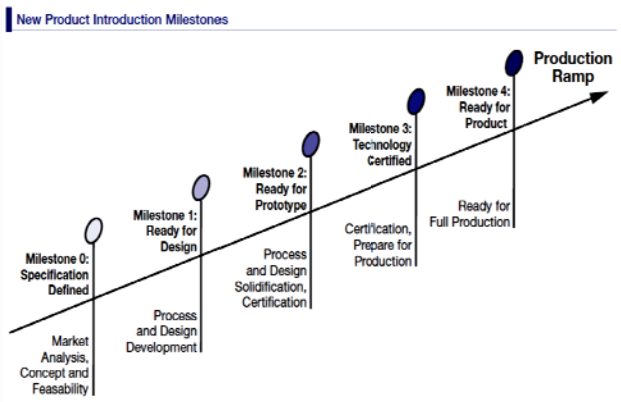
An increase in customer demand for higher quality has triggered Freescale to rethink its quality strategy. The quality legacy embedded in our products goes back to well-known Motorola quality initiatives such as 6-Sigma and Zero Defect. Our customers expect the highest quality from us. Recently Freescale has enhanced its quality strategy in many areas including incident reduction, flawless new product introductions, 1st pass qualification success, rapid problem resolution, and improved quality system processes. In the pursuit of total customer loyalty, Freescale has installed a global, high quality culture that results in manufacturing excellence across all areas. As Freescale continues developing and supporting GaAs products for the wireless infrastructure markets, it was necessary to adopt this new high quality transformation. The major shift in culture was the change from detection and correction proficiency to defect prevention methodologies. The process starts with the adoption of a rigorous NPI phase gate methodology, continues with a comprehensive product qualification process, the execution of product safe launch, and ends with a continuous monitoring by product engineering sustaining group. This initiative is aligned with our customers' expectations and it has been driven from our top executives to every employee in the corporation.

We are not only focused on quality of our GaAs products at the time of purchase, but are also concerned about product reliability as our products are used in specific tiers and environments over time. Freescale product reliability rests on a strong foundation of proven validation principles. Our pre-qualification efforts include designing, modeling, testing and test vehicle investigations to drive low-risk manufacturing processes, providing a proven path to the highest quality.

NPI PHASE GATE METHODOLOGY

NPI methodology is based on a phased process where required criteria are applied before moving to a new phase. Freescale technical and business community form the council that manages entrance and exit of each phase. Figure 1 shows product path from concept to production ramp.

The goal is to minimize risks, account for possible failure modes, design for reliability and manufacturability. The challenge is to maintain the flow to meet time-to-market without attenuating the importance of moving from each phase into the next with solid results and build-in reliability.



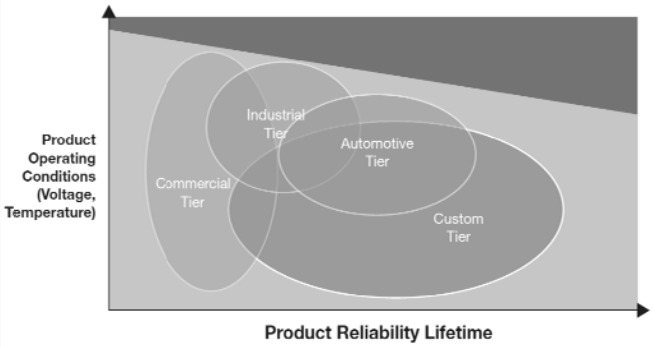
Source: Freescale Reliability Quality Handbook

Figure 1: NPI Milestones

PRODUCT QUALIFICATION

The complexities of new product introduction not only depend on the technology or the application of the product but a complete understanding of the market where the product will compete. The market is commonly divided in tiers: commercial, industrial, and automotive. Each tier has its own set of requirements that need to be understood to ensure alignment from wafer fab to final test. One of the most important factors is the reliability requirements. As the product moves up in the tiers, the reliability expectations increase. Product functionality life time is more demanding in challenging environments. In order to appropriately assess product reliability over a range of product

applications, Freescale follows industrial tier reliability requirements as defined by the Joint Electron Device Engineering Council (JEDEC) and other industry standards. The operating conditions (power, temperature, life time) and reliability requirements (early failure rate, failures in time and wear out) are the main factors during product qualification. Figure 2 shows product operating conditions and reliability lifetime for most common product tiers.



Source: Freescale Reliability Quality Handbook

Figure 2: Product Operating Conditions

Freescale moved away from screened reliability to a build in reliability approach. Starting at product concept, reliability requirements are defined and driven into the subsequent product development phases. The reliability test process starts at the early product phase (prequalification) and continues throughout each phase of the product development. At product qualification reliability is checked but the risk has been minimized by understanding the risks at infant stage and building in reliability in the requirements. A zero failure constraint applies for all conditions tested during the qualification phase.

Freescale uses industry standard accelerated stress test to assess product reliability. Table 1 shows the typical battery of test performed during new product introduction including pre-stress requirements accelerated environmental stresses, accelerated operating life simulation, package assembly integrity, electrical verification, and ESD classification.

PRODUCT SAFE LAUNCH

Safe Launch is a verification of product and process robustness and reliability. The safe launch concept was originally introduced by the Automotive Council as an initiative to ensure product quality. Safe Launch is normally implemented in early production to minimize risk of new parts assumed to be acceptable in meeting customer requirements. It provides documented evidence of process stability baseline. The purpose of Product Manufacturing

Table 1: Typical Qualification Test Plan

JESD MilStd750	Test Conditions	End Point Requirements
PRE-STRESS REQUIREMENTS		
A113	**Preconditioning (PC)** MSL at 260°C, +5/-0°C	TEST DC and RF CSAM - 1008Hrs
ACCELERATED ENVIRONMENTAL STRESS TESTS		
A101	**Temperature-Humidity-Bias (THB):** PC before THB if required. Bias 80% max. 85°C/85%RH for 1008hrs.	TEST DC and RF CSAM - 1008Hrs
A101	**High Temperature and High Humidity (H3T):** 85°C/85%RH for 1008hrs.	TEST DC and RF CSAM - 1008Hrs
A104	**Temperature Cycle (TC):** PC before TC if required. TC = -65°C to +150°C for 1000 cycles.	TEST DC and RF CSAM - 1000 cycles
A103	**High Temp Storege Life (HTSL):** Ta = 150°C for 1008hrs	TEST DC and RF CSAM - 1008Hrs
ACCELERATED LIFETIME SIMULATION TESTS		
A108	**High Temperature Operating Life (HTOL):** Ta=150°C Dev @ max Tj for 1008hrs	TEST DC and RF - 1008Hrs
1036	**Intermittent Operating Life (IOL)** 5000 Cycles. Bias @ max. rating Ta=150°C Dev @ max Tj for 1008hrs	TEST DC and RF- - 5000 cycles
1042	**High Temperature Reverse Bias (HTRB):** Ta= +150°C for 504 & 1,008hrs.; Bias = 80% of max. rated BV	TEST DC and RF- - 1008Hrs
1042	**High Temperature Gate Bias (HTGB):** Ta= +150°C for 504 & 1,008hrs.; Bias = 80% of max. rated Vgs	TEST DC and RF- - 1008Hrs
PACKAGE ASSEMBLY INTEGRITY TESTS		
FSL	**Design Rule Check**	
FSL	**Die Attach Check (CSAM)**	
FSL	**Thermal Resistance**	
FSL	**Bond Pull Strength**	
B102	**Solderability (SD):**	
B100	**Physical Dimensions(PD):**	Cpk ≥ 1.67
ESD AND ELECTRICAL VERIFICATION TESTS		
A114	**ElectroStatic Discharge/ Human Body Model Classification (HBM):** Test @ 250/500/1000/2000/3000 Volts	Test DC and RF
A115	**ElectroStatic Discharge/ Machine Model Classification (MM):** Test @ 50/100/200/400/500 Volts	Test DC and RF
C101	**ElectroStatic Discharge/ Charged Device Model Classification (CDM):** Test @ 200/500/750/1000/2000 Volts	Test DC and RF
Freescale Spec	**Electrical Distribution (ED)**	Test DC and RF - Cpk ≥ 1.67

Safe Launch is to minimize quality risks during new product production ramps. A core team leader is assigned the responsibility of ensuring that the appropriate elements of the safe launch plan (SLP) are implemented on qualification, risk production, as applicable, and production builds. A core team (device, package, product, and assembly engineering)

is formed to review available data from Safe Launch implementation and update Safe Launch plan as appropriate. This methodology requires a detailed plan of the best practices to include increased sample size, increased frequency, enhanced inspection methodologies, phase gates, and most importantly the exit criteria. The core team is also responsible for creating reaction plans such as material review board specifications for non-conforming material (maverick) disposition. In some cases the non-conforming material review can be quite extensive and complex in order to ensure quality and long term product reliability. Another common quality gate is to establish minimum yield requirements at each of the key steps of the fabrication, assembly, and test. Well designed triggering factors for non-conformities can detect potential defects before the product progresses too far down the manufacturing line. And finally, a direct communication with the fab, assembly, and test factories brings SLP to execution. The core team has a primary task to promote these initiatives to each party. In addition, the core team needs to continuously visit (audit) each site to ensure that the communication is direct and each party conforms to the plan and understand the importance of the execution phase. Communication is the key for a complex process such as Safe Launch. Success depends on each and every step. A single mishandling could potentially setback the entire initiative. Table 2 shows a sample safe launch plan.

Table 2: Safe Launch Plan

Process Name/ Operation Description	Where	Potential Failure Mode	Evaluation Technique
Reliability Test	Overall Process Flow	ALL	Identify additional monitors
GaAs Fabrication	Wafer Fab	EPI Defectivity	Incoming inspection data
GaAs Fabrication	Wafer Fab	Field life failure; parametric test yield	Data from EPI supplier
GaAs Fabrication	Wafer Fab	Early w earout	Perform life reliaiblity testing
GaAs Fabrication	Wafer Fab	Excessive Process Variation	SPC
GaAs Fabrication	Wafer Fab	Non-conforming Material	Core team disposition
GaAs Fabrication	Wafer Fab	Die thickness variation	SPC
Via Process	Wafer Fab	Delamination	SPC
Auto Vision Inspection	Wafer Fab	Defects	SPC
GaAs Fabrication	Wafer Fab	Unforseen process change	Core team review
Package Design	Assembly	ALL	DRC
Assembly CZ	Assy Site	ALL, special focus on MSL	Review monitors
Die Bond	Assy Site	Die crack, chip, broken die	Review SPC monitors
Die Bond	Assy Site	Die crack, periphery non-w etting, epoxy on die	Review SPC monitors
Diebond	Assy Site	Die Attach Voids / Poor Coverage	Review SPC monitors
Wire Bond	Assy Site	Poor Ballbond Placement, Die crack	Review SPC monitors
Wire Bond	Assy Site	Poor Ballbond Integrity	Review SPC monitors
Singulation	Assy Site	Package defects	Review SPC monitors
Singulation	Assy Site	Delamination	Review CSAM monitors
Final Test	Production Test	DC and/or RF failures (marginality)	Review distributions
Failure Analysis of FT fallout	Production Test	All Failures	Failure analysis
100% QC Gate	Production Test	Test Process Escape	Review records
Reliability Assessment Monitoring Plan	QA Lab	CSAM, Electrical Test, Die Attach, Wirebond Analysis, MSL	
Review of Safe Launch Results	Overall Process Flow	Systemic Issues	
Overall Review of CQI for Systemic Issues	Overall Process Flow	Systemic Issues	

PRODUCT SUSTAINING

In order to increase our GaAs product quality we built on the Freescale global quality initiative and holistically added one more layer to further reduce the risk of failure. The failure rate of semiconductors is inherently low; therefore, the GaAs quality team strongly believes in a balance between fixing the fundamental problems impacting quality during the design phase, and deploying procedures and inspections as best practices to detect low level quality incidents. Our approach starts at the front end (wafer fab) and moves step by step to the back end (assembly, final test and distribution). It is difficult for fab engineers to get exposure to the entire process of developing a new product in particular the assembly challenges. Educating fab engineers on the key assembly factors plays an important role in the success of manufacturing high quality products. GaAs products in particular carry many challenges due to the intrinsic brittleness of the compound material and the immaturity of the assembly processes. Continuous feedback from product engineering can proactively benefit new product introductions by eliminating gaps and bringing awareness to the fab. One example is the impact of dicing methodologies on the die strength and die crack avoidance. Another is the consistency of die thickness (grind repeatability) as a major driver of bond line thickness especially for thin die (≤3mil). In a similar case, product engineers do not have exposure to the complexities of fab processes. Without exposure to the fab it is not easy to understand that changes in fab processes carry tremendous risk of introducing variances. Product engineers are more familiar with final manufacturing and final test as opposed to the complexities of fab processes. Another layer of complexity is the assembly engineer view of the fab and product combination. Freescale GaAs products are often assembled at external factories that have extensive experience dealing with Si products but limited GaAs assembly experience. GaAs, being lower volume, generates many challenges that translate into many risks. A proactive position to educate assembly engineers in the intrinsic characteristics of GaAs (a material with much lower fracture

strength than Si and poor heat transfer requiring very thin die) can avoid long term reliability issues due to unnecessary induced stresses during assembly. Our approach is to make the product engineer the liaison for fab and assembly; it is a great advantage when the product engineer is the binding element of the entire manufacturing process.

One of the areas where we concentrate efforts to reduce quality risk is during assembly. The nature of the compound material requires special handling and awareness. We deployed enhanced assembly control plans as a form of best practices targeting specific areas where unwanted stresses are introduced. For example die bond coverage is an important parameter and we need to ensure that the bonding material does not leave voids evolving as stresses concentrators. Package trimming can be another area where GaAs die can be stressed if the process is not adequately controlled and monitored accordingly. Table 3 shows an example of best assembly practices deployed at sub-cons. Each group of inspections is tailored depending on the site capabilities, resources, and tool sets.

Table 3: Best Assembly Practices

Assembly Site	SITE A	SITE B	SITE C	LEGEND
Wafer Level Unit Probe	100% Test	100% test	100% Test	FAB Practice
FAB Final outgoing inspection	AUTO VISUAL 100%	AUT) VISUAL 100%	AUTO VISUAL 100%	Best Practice
Incoming Wafer Inspection	Visual 100X	Visual 100X	Visual 100X	Special
Additional Die Crack Visual Inspection	Visual 200x	Visual 200x	Visual 200x	Standard Practice
Die Bond Inspection	Visual, 100-200x for 80% periphery (90% coverage)	Visual 50x-200X for 80% periphery (90% coverage)	XRAY (90% coverage) and visual for 80% periphery	
Additional Die Crack Visual Inspection	Visual 200x	Visual 200x	Visual 200x	
Wire Bond Inspection	Die Inspection for cracks, sample wire pull & ball shear	Die Inspection for cracks, sample wire pull & ball shear	Die Inspection for cracks, sample wire pull & ball shear	
Additional Die Crack Visual Inspection	Visual for die cracks	Visual die cracks	Visual die cracks @ 200x	
Post-mold inspection	X-Ray/CSAM 5% single 10% total	Visual & X-Ray for wire break / sweep	Visual and X-Ray for for 5% max single void, 90% coverage	
Post-trim inspection	CSAM / and decap for die crack inspection	External visual for dimension check	External visual	
Convection or IR oven 1x Reflow (260°C) before FT	Convection oven Reflow	IR Reflow	IR Reflow	
Finished goods sample inspection	Decap + Visual Inspect 100X	Visual inspection + Lead Peel Test @ 95% coverage	Decap + Visual inspection + X-Ray (general die bond quality)	
Compliance Matrix Control Plan PFMEA	Adherence to enhanced Ctrl Plan and FMEA	Adherence to enhanced Ctrl Plan and FMEA	Adherence to enhanced Ctrl Plan and FMEA	
Finalt Test	100 % test + zero failure QA gate	100 % test + zero failure QA gate	100 % test + sample retest (LTPD 1%) + zero failure QA gate	
Enhanced MRB/MTY/Safe Launch	MRB/MTY/Safe Launch	MRB/MTY/Safe Launch	MRB/MTY/Safe Launch	

RESULTS AND CONCLUSION

Freescale GaAs quality team has been able to deploy these initiatives from wafer foundry to multiple external assemblies and test sites. The success has been significant as seen on an exponential decline of customer quality incidents of GaAs products as shown on Figure 3. The key factors have been built in reliability, clear expectations in the product qualification process with a zero failure criteria, the execution of the safe launch program, and the communication stream amongst all parties. Freescale GaAs team has launched multiple products to the satisfaction of the customers, always ensuring the highest quality and proven reliability.

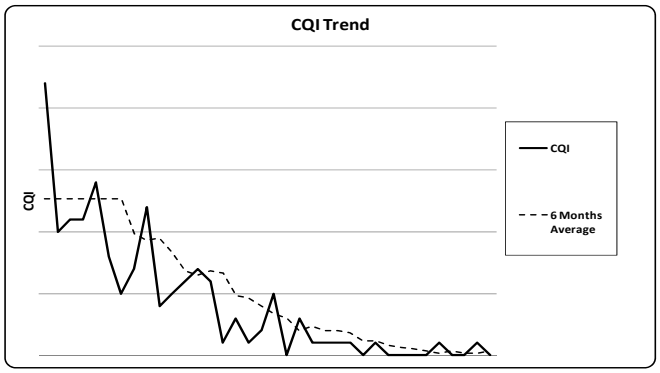


Figure 3: GaAs Products Customer Quality Incident Trend

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ACRONYMS

CZ: Characterization
NPI: New Product Introduction
SLP: Safe Launch Program
CSAM: C-Mode Scanning Acoustic Microscopy
THB: Temperature humidity bias
HTOL: High temperature operating life
TC: Temperature cycles
ESD: Electrostatic discharge
HBM: Human body model
MM: Machine model
CDM: Charge distribution model
HTRB: High temperature reverse bias
HTGB: High temperature gate bias
H3T: High temperature high humidity
IOL: Intermitting operation life
MSL: Moister sensitivity level
MRB: Material Revision Board
MTY: Minimum Test Yield