Germanium and compound semiconductor manufacturing for advanced CMOS

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Abstract

The present work presents a review of the progress in all parts of high mobility (Ge and III-V) advanced CMOS, from the engineered substrates and co-integration schemes, to the channel device structure the gate dielectric and the source and drain contacts. The aim is to identify the main challenges and the prospective solutions which will allow the manufacturing in a Si-compatible flow for volume production.

INTRODUCTION

The world is rapidly moving into the mobile information age were mobile internet devices (MID) like tablets and smartphones are at the center of attention for consumers, integrated device manufacturers and technology developers. For MIDs and other multimedia applications, control of power consumption at an acceptable level without losing speed is an important requirement. To fulfill this requirement, transistors are made to operate at low power supply voltage, which however leads to performance degradation. Performance boosters such as strained silicon have been extensively used until now, but they are already out of steam so that new solutions are urgently needed. Germanium and III-V compound semiconductors come at a rescue, offering high carrier mobility for the replacement of silicon in the transistor channel to manufacture the next generation advanced CMOS. At present, there is no clear material winner, however a dual channel solution is favored in which p FETs comprise Ge (SiGe) channel while n FETs require InGaAs channel materials [1,2].

MAIN CHALLENGES

1) Co-integration on large area Si substrates: The main technological challenge is the co-integration of the dissimilar channel materials on the same large area (300 mm or larger) Si substrate in a scalable and manufacturable process which will ensure volume production. There are two main routes (Fig. 1) for co-integration: (a) direct growth on bulk Si via a selective heteroepitaxial growth, (b) semiconductor-on-insulator approach. The obvious advantage of the first approach is its compatibility with Si CMOS manufacturing, low cost and IP re-use. On the other hand, the second approach offers better electrostatic control of the channel, an important requirement to maintain performance in aggressively scaled devices.

Fig. 1 Schematic representation of dual channel CMOS (a) integration on bulk Si (b) semiconductor-on-insulator integration scheme. QW denotes the Ge and InGaAs quantum well channel. BOX stands for buried oxide isolation and GOI stands for germanium on insulator.

The focus here is on the first approach, which suffers from the well-known problems of heteroepitaxy of III-V compounds on silicon such as antiphase domains (APD), misfit and threading dislocations and thermal stress. We discuss one of the possible solutions, using Aspect Ratio Trapping (ART) technology [3]. The latter takes advantage of the well known “necking” effect during growth on patterned substrates where threading dislocations and other defects are confined at the bottom of deep and narrow trenches leaving the top part defect free for device definition. As technology progresses to smaller dimensions, ART becomes more effective and more important. As shown in Fig. 2, the fabrication of ART-engineered substrates starts with standard STI Si wafers followed by etching to define the narrow trenches. A key enabler is the selective epitaxy of Ge and III-V semiconductors by MOCVD to fill the trenches and produce high quality channel layers. A last chemical and mechanical polishing (CMP) step is needed in order to level-off the grown structures and produce smooth surface morphologies. Filling the trenches with good quality III-V device layers is challenging.

In a process pioneered by imec, a Ge starting/seed layer is deposited directly on Si (Figs. 2 and 3) offering better compatibility with the MOCVD reactor growth processes...
facilitating also the local formation of double-stepped misoriented surfaces in the trench so as to minimize APDs.

Fig. 2. Process sequence for the co-integration of Ge and III-V devices on the same ART-engineered Si substrates using selective epitaxy in deep and narrow STI trenches

An InP buffer with or without a lattice matched InAlAs barrier followed by a lattice matched (In composition of 53%) InGaAs channel layer and a dielectric/metal gate stack complete the device layer structure (Fig. 3).

Most defects are trapped at the bottom of the trenches [4] and their density and propagation through the top active channel layer are minimized (Fig. 3). During the early development stage, severe faceting in the channel was observed which is progressively getting under control. First generation of functional n-FETs give satisfactorily high ON-state currents indicating that the channel is of sufficient quality. However, the OFF-state current is way too high hampering transistor performance. While reduction of defectivity in the channel (dislocations and other defects) is always the first priority, leakage currents through the InP or InP/InAlAs buffer or through the Si substrate is an additional big problem requiring an intense effort to find appropriate solution.

Substantial innovations in the MOCVD tools are essential with regard to the susceptor design for temperature homogeneity, exhaust configuration for particle reduction and lower process pressures, and quartz cover plate design for uniform showerhead temperature and particle reduction. These features ensure good selectivity and make the equipment compatible with large area (300 mm) wafer processing in compliance with the strict contamination avoidance rules of existing Si CMOS processing lines.

2) Surface passivation and ultrathin gate dielectrics. A second important challenge is to develop suitable surface passivation methodologies and gate dielectrics which should be preferably common for both Ge (SiGe) pFET and InGaAs nFET to minimize manufacturing complexity [5]. This has been demonstrated by imec using sulfur passivated Ge and InGaAs surfaces followed by rather thick (8-10 nm) Al2O3 gate dielectrics (Fig. 4).

Fig. 3. Imec data, partly published in Ref [4]. SEM micrographs showing in cross-section (a), (b) and top view (c) a III-V device layer structure selectively grown in a narrow and deep trench on Silicon. The Ge starting/seed layer, the InP buffer and the InGaAs active channel are shown in (a).

Fig. 4. After Ref. [5]. High frequency Capacitance-Voltage curves of MOSCAPs with 8-10 nm Al2O3 gate dielectrics on Sulfur- treated surfaces for InGaAs nMOS (a) and Ge pMOS (b) devices, showing symmetric behavior with minimum frequency dispersion in accumulation. The bottom graph shows the interface density of states Dit in the energy gap.
Although sulfur-passivated Al₂O₃ gate could be suitable for both type of devices (Ge pMOS and InGaAs nMOS) scaling to low enough equivalent oxide thickness (EOT) may be challenging, therefore optimization research is on-going. The research for gate dielectrics for Ge MOS devices has matured although a suitable gate dielectric has not been selected yet. The consensus is that a good quality GeO₂ (or GeOₓ) is essential at least as a thin interfacial layer followed by a metal oxide cap layer. The situation is less clear for InGaAs MOS devices, since the MOS capacitor device characteristics are far from ideal in most cases, for reasons which are not fully understood. Nevertheless, satisfactory InGaAs MOSFETs with relaxed EOT (~2.2 nm) have been demonstrated [6] indicating that gate dielectrics do not present a fundamental problem. The biggest challenge at present is to scale the dielectric to low EOT values (1 nm or lower) as required, without jeopardizing the interface quality between the dielectric and the semiconductor. Perhaps the most promising solution is proposed by U. Tokyo researchers [7] for Ge MOS: A 1-1.5 nm thick Al₂O₃ layer is first deposited by ALD followed by post oxidation treatment using an ECR plasma source which produces an ultrathin GeOₓ interfacial layer controlled by the Al₂O₃ oxidation barrier thickness. A good compromise between interface quality and low EOT is obtained at a GeOₓ thickness of 0.5 nm yielding ~1 nm EOT Ge p-MOSFETs with very good mobilities ~437-526 cm²/Vs.

3) Self-aligned S/D regions and metal contacts. A third important challenge is to develop very high quality ohmic contacts for the source and drain regions for both types of FETs [8]. The contacts should meet the stringent technology requirements targeting specific contact resistance Rₓ less than 10⁻⁸ Ω-cm² and a sheet resistance Rₛ < 21 Ω/sq for technology nodes beyond 22 nm.

In metal/semiconductor junctions, the electron barrier height φₛₓ is connected to the pinning factor S, the metal work function φₛ, the semiconductor affinity φₛ, and the charge neutrality level φₓ via \[ \phi_{S,x} = S(\phi_S - \phi_{CNL}) + (\phi_{CNL} - \chi) \]. S=1 represents the ideal Schottky limit where \( \phi_{S,x} \) varies linearly with \( \phi_S \), while S=0 represents the Bardeen strong pinning case where \( \phi_{S,x} \) is essentially independent of the metal workfunction [8]. In Ge the Fermi level is strongly pinned (S factor ~0.05-0.02) very close to the CNL which is only 0.08-0.09 eV above the top of the valence band (VB) (see Fig. 5) [9]. This means that the Schottky barrier height for holes is very small facilitating the formation of good ohmic contacts in p-type S/D regions for Ge p-FETs. Similarly, good ohmic contacts for InGaAs n-FETs are favored due to a small Schottky barrier of electrons at metal/n-type InGaAs interfaces.

The biggest challenge is to fabricate the contacts in a self-aligned way and in a Si CMOS compatible flow to ensure the lateral scaling of these devices to gate lengths lower than 20 nm as required for the future technology nodes. For the case of Ge a self-aligned definition is typically achieved by blanket metal (e.g. Ni) deposition over the device area, followed by annealing at higher temperature to form NiGe alloy on the exposed S/D regions, and subsequently removing the unreacted Ni over the gate or other places of the transistor by selective etching (Fig. 6) [10]. Self-aligned NiGe contacts developed and optimized by imec have given low Rₓ ~9 Ω/sq and state of the art short channel Ge (65nm) [11] pFETs with very good performance.

Fig. 6. After Ref. [10]. SEM micrograph showing (a) germande overgrowth on isolation areas and massive voiding after a one-step RTP and (b) improved contacts after a two-step optimized RTP.

For the case of InGaAs n-FETs, it is less clear at present whether a self-aligned S/D and “silicide-like” metal contact technology can be implemented at short channel lengths. Nevertheless, significant progress has been made by several groups [12, 13] focusing on Ni-InGaAs alloy (“nickelide”) contacts which offer low Rₓ (~25 Ω/sq) as already shown by researchers at Tokyo U [12]. Very recently, researchers at IBM-Zurich [13] have demonstrated MOVPE-grown raised n+ InGaAs S/D regions of high crystalline quality with excellent growth selectivity over the gate area. Self-aligned
Ni-InGaAs metal contacts were realized [13] with optimized process conditions leading to $R_s=16.3 \, \Omega/$sq and $R_p=105 \, \Omega$-$\mu$m², although $R_p$ is still two orders of magnitude larger than that expected for 11 nm node technology. Electrical properties have been demonstrated to be stable up to 500°C making this process suitable for standard BEOL/interconnect processing. It is worth noting that the raised S/D regions and contact formation are compatible with ET-III-V-OI integration platform (Fig. 1(b)). Finally, long channel (15µm) FETs made with Ni-InGaAs contacting scheme show satisfactory performance characteristics with only slight degradation observed after alloy forming temperature treatment. The specific contact resistance needs to be further reduced by increasing n+ InGaAs doping to meet specifications for advanced nodes. Shorter channel FETs in the 10nm scale need to be fabricated to prove suitability for self-aligned processing.

**CONCLUSIONS**

Development of high mobility (Ge and III-V) dual channel CMOS faces some important challenges. First, co-integration on ART-engineered Si substrates faces the problems of heteroepitaxy. Although facetting and threading defects in the InGaAs channel have been minimized, excess OFF-state leakage through the InP buffer (or Si substrate), hampers transistor performance. Second, in the area of gate dielectrics, combining good quality surface passivation with low EOT (~1nm) is a challenge, however it is not considered as a show stopper and significant progress has been demonstrated. Defining S/D regions and low specific contact resistance metal contacts in a self aligned way, is a third difficult challenge which is currently faced using NiGe and Ni-InGaAs alloy contact technology for Ge pFET and InGaAS nFET respectively.

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**ACRONYMS**

MID: Mobile Internet Devices
FET: Field Effect Transistors
CMOS: Complementary Metal-Oxide- Semiconductor
ART: Aspect Ratio Trapping
STI: Shallow Trench Isolation
APD: Antiphase Domains
CMP: Chemical and Mechanical Polishing
MOCVD: Metal Organic Chemical Vapor Deposition
EOT: Equivalent Oxide Thickness
CNL: Charge Neutrality Level
RTP: Rapid Thermal Processing
ALD: Atomic Layer Deposition
S/D: Source-Drain
ET-III-V-OI: Extremely thin III-V on Insulator.
BEOL: Back-End of Line