Manufacturing of Cu-pillar Bump for III-V MMIC Thermal Management

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Abstract

Cu-pillar bump manufacturing technology applied to III-V MMIC thermal management is reported. IBM C4 technology has been used in high volume production on CMOS wafers for several decades. In addition to smaller real estate on PCB, when coupled with the corresponding flipchip packaging structures, better performance in both thermal and electrical characteristics could be expected from bumped chips especially when the application power or application frequencies are high. When coping with higher thermal density and flexible thermal source distribution, Cu-pillar bump design outclasses the solder bump structure which is prevailing in CMOS community. However there were several potential obstacles for the manufacturing of Cu-pillar bump structures on GaAs wafers, including the brittleness of the substrates, thermal bar design induced extra bump coplanarity, and the productivity problem due to low copper deposition rate. Approaches to solve these potential issues are addressed in this report.

INTRODUCTION

IBM C4 (controlled-collapse chip connection) technology has been utilized in high volume production for decades and millions of wafers are bumped every year now. Since C4 chips are flipped to make connection with chip carriers when doing IC packaging assembly, people often refer to it as flipchip technology. Ceramic chip carriers, plastic chip carriers, and metal chip carriers have been successfully utilized to assemble bumped die for different purposes. Comparing to its counterpart, the chip with wire bonding connections, the C4 chip take smaller real estate on chip carrier since the interconnections take place under the chip itself, not like wire-bond chips, the interconnections start from the final metal pads of the chip and end at the bond pads which locate outside of the projection of the chips on the chip carriers. Since it is possible to use an area as small as the chip size to design a chip carrier for the bumped chips, and sometimes the bumped chips can be mounted on system board directly, thus bumped chips are referred as real CSP (chip scale package) sometimes. The dimension shrinkage of interconnection between the chip and the chip carrier in flipchip packaging makes it another merit since it has shorter and fixed interconnection with wider cross-sections. This makes the electrical performances of C4 chips easier to be predicted and often be better than its counterpart. Another merit of flipchip packaging is that it reduces the thermal resistance between the packaged chips and the ambient, this is because the major thermal path in flipchip package does not have to go through any low thermal conductivity material like molding compound or die attach glue, which increases the thermal resistance for IC packages. In the early stage of C4 technology, metal evaporating technology was adopted to deposit solder on bumped wafers, as time moves on it was replaced by either plating technology or printing technology to deposit the solder alloy metal. Although plating is used as the mainstream technology to produce bumps, printing technology is also popular in the industry because it is easier on process control and it costs less to process. To meet RoHS requirements, leadless tin alloy or pure tin are often adopted for solder bump manufacturing, few people choose Cu-pillar bump to meet RoHS criteria due to its productivity and cost. Consequently people usually choose Cu-pillar bumps rather than solder bumps only in the cases that better performance or flexible geometry shape of the bumps counts, for example when better thermal performance or non-sphere shape bumps are required in the applications. Recent plating chemical developments make it possible to raise the throughput of Cu-pillar bump and make it possible to reduce its manufacturing cost. The authors have compared different chemicals to reach a suitable BOM for decent cost of Cu-pillar bump process. Flipchip technology is relatively new for compound semiconductor wafers, thus several potential issues were expected for Cu-pillar bump manufacturing, the authors have successfully solved those potential issues and the approaches are depicted in this article.

BRITTLENESS OF SUBSTRATES

Due to its brittleness, wafer breakage is one of the major factors to reduce the process yield of GaAs wafers and it occurs when the summation of the applied stress and residual stresses exceeds the fracture strength of the substrate[1]. Even changes in thermal ramp have impacts on wafer breakage rates[2]. Thinner wafers are easier to be broken during the process and handling and thus special process design are needed to handle thinned wafers[3,4]. Few bumping facilities have successfully duplicated their

existing experience on GaAs wafers. One of the major obstacles is the wafer breakage rate. Statistical numbers (Earlier data) [5] show initial wafer breakage rates are as high as 15-25% at the beginning stage when outsourcing to a new bump facilities.

In addition to higher risk to process with thinned wafers [3,4], the temperature profile for solder reflow also needs to be modified to get smooth solder cap as people usually expect. The adhesion material between thinned wafers and wafer carriers needs to survive the PR removal chemical during the PR striping process which is following the plating metal deposition process. Since the PR used in Cu-pillar bump process is designed to survive plating chemical under long process time without being lifted or dissolved in the plating chemical. Thus PR stripping chemical is designed to be so strong that few materials can survive its attack. Several adhesion materials have been tried but all of them were at least partially lifted as shown in Figure 1. Thus full thickness wafers were preferred by the authors to go through bump process.

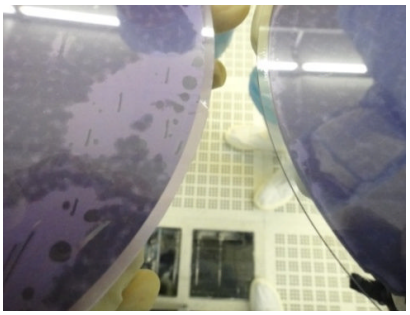


Figure 1. Chemical attack on adhesion materials after PR stripping process.

A typical Cu-pillar bump process flow is depicted in Figure 2 with full thickness. The authors used this process flow to go through the studied for the remaining part of this article.

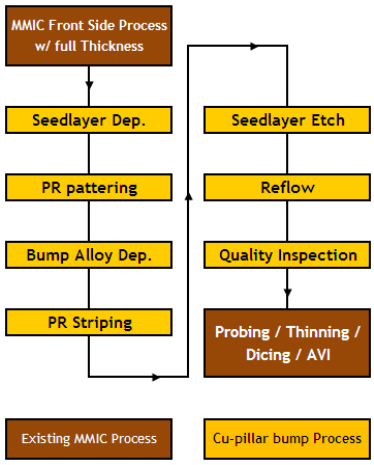


Figure 2. Typical Cu-pillar bump process flow

Selection of suitable process tools and associated process recipes can help to reduce wafer breakage rate. Contact forces and agitation need to be arranged not to exceed the accumulated stress limit for the substrate. It is believed that the agitation during long distance shipping would contribute to wafer breakage rate, thus it is suggested to have GaAs wafers bumped at the same site that transistors are manufactures.

THERMAL BARS AND IN-DIE COPLANARITY

Almost all the bumped wafers in the silicon community have only one bump size in the same chip. Bump heights uniformity in the wafers can usually be controlled by adjusting the electrical field and chemical flow (in the plating process). Bump height distribution and bump height difference in the wafers are usually a function of the specific plating tool. However, the requirement for even thermal dissipation for adjacent heat sources and the high thermal density design make it necessary to have different bump sizes in the same chip in order to have major heat source in the die to be covered under the thermal bar. Figure 3 shows a bump layout design with large thermal bars on top of major heat sources to make the chip's thermal resistance lower than that of traditional chip design, and consequently much better thermal performance can be expected.

Figure 3. A Cu-pillar bump layout with thermal bars in the chip. Thermal bar can improve heat dissipation to ensure the chip's performance.

In-die coplanarity has not been a concern for bump manufacture since it was automatically solved whenever in-wafer coplanarity meets the criteria. Criteria for in-die coplanarity or in-wafer coplanarity were used to gate the bump heights so that the bumped chip can be successfully assembled without any bumps not been well connected with the pads on the chip carriers. However, when there are multiple bump sizes in the same chip, in-die coplanarity would be an potential concern since Cu deposition rate is an function of the aspect ratio of PR opening [6], and thus different bump size will result in different deposition rate or bump height in the same die. When the range of bump height within a chip, *i.e*, in-die coplanarity, exceeds the limit of tolerance for downstream flipchip assembly capability, the packaging assembly houses would not be able to complete the packaging without failures.

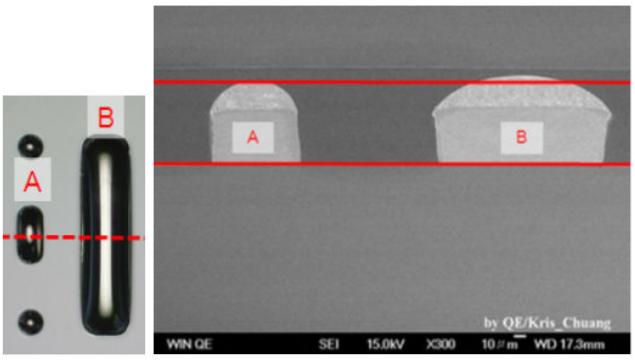


Figure 4. Cross-section shows different bump heights can be expected from different bump sizes although they are in the same chip.

Figure 4 shows the difference in bump height for different bump size from a typical process. Several approaches can be used to solve this problem, for example, the deposited metals can be etched back or milled back to the same bump height before sending the wafers to go through reflow oven. Depositing Cu or solder on selected bumps at one stage, and then use multiple plating stages to receive the same bump height in the same chip. The above two approaches should be able to apply to all kinds of chip designs after database is generated. However, the most economic approach is to enhance agitation and chemical flow to reduce the difference in plating boundary layers thickness of different bumps, however, theoretically there are always differences in the plating boundary layers on the surface of cathode, thus this approach can only reduce but not eliminate the difference in plating boundary layer thicknesses, and the result could be different from mask to mask due to bump layout design would be different from one chip design to another.

"No reflow before dicing" is another way to reduce the impact of in-die coplanarity issues. Figure 5 shows some measured bump heights of a bumped wafer before and after solder reflow process. Total of 450 thermal bars and 3150 bumps from 450 die are measured in 9 regions of the wafer; measurements are made before and after reflow process. The plot in Figure 5 shows bump height increases after reflow process, this is due to the solder cap deforms from a short cylinder (before reflow process) to a dorm (after reflow process) as shown in Figure 6, and this deformation makes bump height grow 7.9 um in average as shown in the left hand side of Figure 5. On the right hand side of Figure 5, the plot shows average 10 um increases at bump height during the solder reflow process for thermal bars. This makes the in-die coplanarity increase at least 2.1um when a thermal bar is there.

The length of a thermal bar is another factor to influence in-die coplanarity. Similar measurements show when a longer thermal bar is in the chip design, the in-die coplanarity will deteriorate at least 6.5 um as shown in Figure 7.

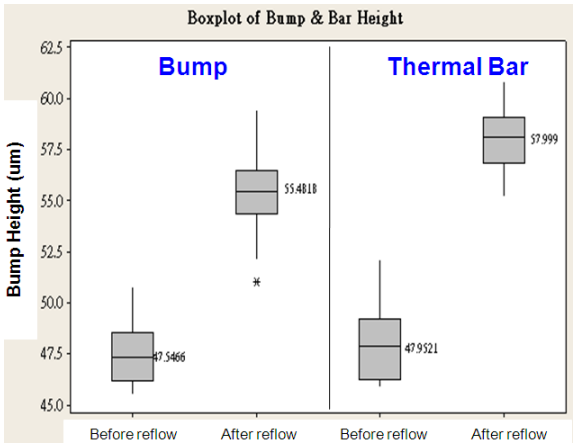
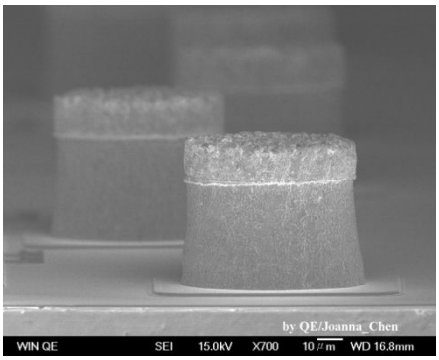
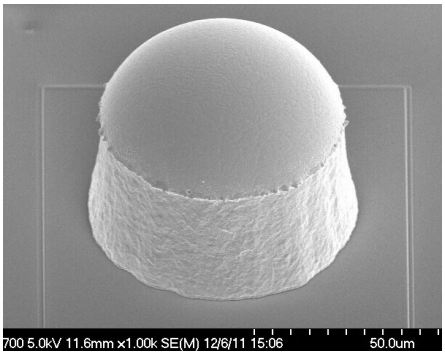


Figure 5. Bump height measured before and after solder reflow process for a chip design with a short thermal bar.



(a) Cu-pillar bump before reflow process



(a) Cu-pillar bump after reflow process

Figure 6. Shape change of solder cap due to solder reflow process

Although it is a potential concern to do flipchip assembly with thermal-bar induced extra in-die coplanarity, data shows there are no issues to have this type of chips with 14 um in-die coplanarity assembled in flipchip packaging. However, if there is a need to eliminate this thermal-bar-induced extra in-die coplanarity, it can be managed to do solder reflow after chips are bonded on chip carriers.

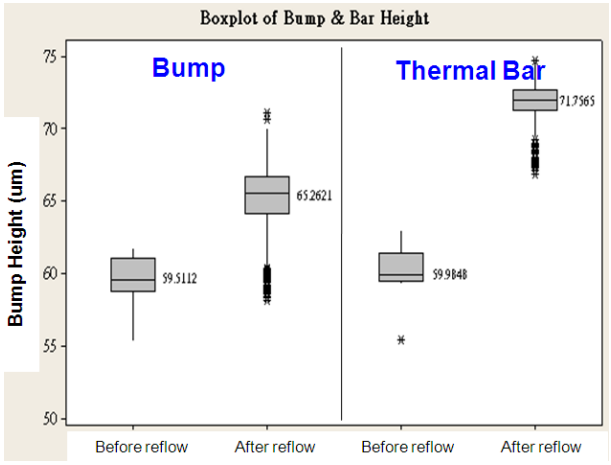


Figure 7. Bump height measured before and after solder reflow process for a chip design with a long thermal bar.

COPPER DEPOSITION RATE

Cu deposition rate is one of the major obstacles for the industry to migrate from solder bump designs to Cu-pillar bump designs. Most of the commercial chemicals are operated at the current density less than 10 ASD in the industry for Cu deposition. If pulse-off scheme is used to enhance Cu deposition quality, a typical process step to deposit Cu pillar only would takes more than one hour. Thus the throughput for Cu-pillar bump process would be dominated by the bottleneck at the Cu-deposition step. In order to reduce the manufacturing cost for Cu-pillar bump process, five sulfuric acid based plating chemicals were compared and verified with Cu-pillar bump process. Every chemical comes with different pros and cons, for example, the chemical provided by vendor D was popular in the industry, however its uniformity is not easy to control when Cu deposition rate goes higher than 2 um/min. In order to achieve more than 800wafer/month from one single plating cup, vendor E's chemical is selected to meet the requirement of high volume manufacture.

TABLE I
Several commercial available Cu-plating chemicals.

Vendor	Base Solution	Max Current Density	Remark
A	H2SO4	12 ASD	Good R&D capability
B	H2SO4	15 ASD	Easy on bath management
C	H2SO4	8 ASD	Low stress
D	H2SO4	20 ASD	Popular in the industry
E	H2SO4	35 ASD	Smooth surface

CONCLUSIONS

Several potential obstacles for Cu-pillar bump manufacturing on III-V MMIC are discussed and have been resolved successfully. When the Cu-pillar bump manufacturing is mature in the industry, designers will move forward to more aggressive design rules with thermal bar designs to solve heat dissipation problems..

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