

Backside Via Process of GaN Device Fabrication

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Abstract

Several backside via integration methods have been tested on GaN device fabrication. Some of the methods create potential reliability issues, due to undesirable chemical attack or poor via profile. An improved process integration method was demonstrated that produces vias with the desired profile and without the same potential reliability issues.

INTRODUCTION

There is considerable and increasing interest in GaN devices for high power application. This is evident in recent volumes of publications on the subject. GaN has high breakdown voltage, high electron mobility and saturation velocity [1], making it an excellent material for many applications including high-power, high speed, and high-temperature microwave applications [2]. For electronic applications, GaN is typically grown on SiC substrate, which itself is a material of great interest for many decades [3].

Both SiC and GaN are strong and durable materials. They are chemically stable, not easily attacked by any acids or alkalis. While these are useful properties that make SiC and GaN devices operable at high temperature, they also introduce some new complexities in device fabrication. For example, for high power MMIC applications, electric connection through backside via is often used to further improve the performance of GaN devices. As GaN is mostly grown on SiC, backside SiC/GaN via etch is thus an essential part of the device fabrication process. For this reason, there have been many studies on SiC substrate via etch in recent years [4-15]. At the present, SiC via etch is still a relatively slow process (~ 1um/min) compared with other materials such as Si or GaAs. As a result, long etch time is often needed to etch through the SiC substrate. This excludes the possibility of using photo-resist as the etch hard mask. Metal hard masks are often used instead. In a typical via formation process, SiC surface is first coated with a layer of metal film outside of intended via area as a hard mask to protect the substrate during via etch. Then SiC is etched in the via area. In the case when SiC is used as a substrate for GaN device, the GaN layer is also etched after SiC via etch is complete. After completing both SiC and GaN etch, the metal hard mask is removed. The metal hard mask is not as easily removed as a photo resist mask.

Often the metal hard mask removal process is performed using wet chemical etch. In one typical process flow, before removing the hard mask, the via is filled with photo resist (or other sacrificial material). The photo resist is used to prevent the chemicals used to remove the metal hard mask from attacking the metal layer under the via. (For convenience of discussion, metal layer under the via is called via etch stop layer, or VES.) However, this via protection method is generally not robust enough. Some chemicals can leak through the photo resist, reach the bottom of via, and attack the VES. This could create voids in the VES and potential via reliability issues.

To avoid chemical etching of VES, alternate integration methods have been tested. This paper reports on the results of some of the tests.

EXPERIMENT

Most of the tests reported in this paper were conducted on 100 mm GaN wafers. All GaN wafers were GaN grown on SiC substrates. VES is composed of primarily two different metals, metal 1 and metal 2 in multiple alternate stacks. After completing the front side device fabrication process, GaN wafers were mounted onto 4 inch carrier wafers, with the circuit side (front side) of GaN wafer making contact with the carriers. The SiC substrate is then ground and polished to its final thickness (typically ~ 100um). A via pattern was formed on the SiC surface with about 60 um via diameter. A metal hard mask was deposited onto SiC surface except where via is to be formed.

For SiC/GaN via etch, inductively coupled plasma (ICP) etch tool with optimized ICP source was used. Details of SiC etch process have been described elsewhere previously [14-15]. Etching process is the same for all tests reported in this paper.

Three different integration methods have been tested: (A) Both SiC and GaN were first etched to open via to VES layer. Then the via is filled with photo resist, followed by metal hard mask removal using wet chemical etch; (B) First, only the SiC was etched, then metal hard mask was removed, followed by GaN etch. In this method, the VES is fully protected by the GaN layer during metal hard mask removal.

Improved VES integrity is expected using this method; (C) Both SiC and GaN were etched, followed by an alternate metal hard mask removal process to remove the hard mask layer. This new alternate hard mask removal process does not use any chemicals that would attack the metal in VES layer. Therefore good VES integrity is also expected.

RESULT

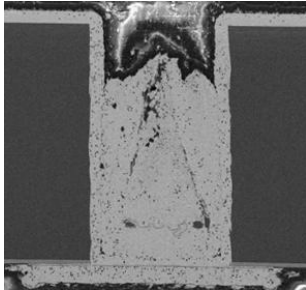


Fig 1 Typical SEM image of via of wafers in group A.

Typical via profile of group (A) is shown in FIG 1. The via is filled with metal during backside metallization process. (Metal seen in the middle of via is an artifact due to sample preparation). This figure shows a very directional via etch, with nearly vertical via side wall. Metal filling of via also appears to be good in this picture. However, when examined in more detail using FIB technique, some defects become clear in some of the via, as shown in FIG. 2. FIG 2a is the FIB cross section of a different via (but within the same group of sample A) at its bottom, and FIG 2b is the magnified view of the same via at its two bottom corners shown in FIG 2a. Voids in the VES layer are visible in FIG 2b.

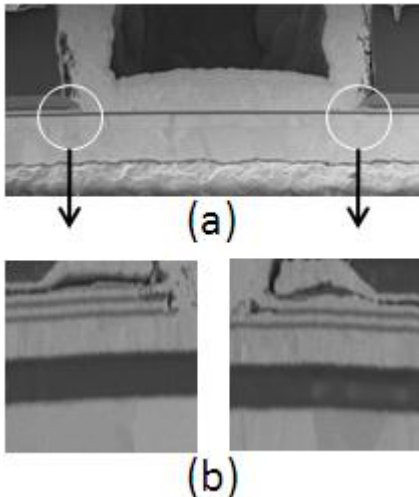


Fig 2 Cross section of via of a wafer in group A. (a) The overall via shape at the bottom of via, (b) magnified view of corners of the via shown in (a).

The voids in FIG 2(b) are likely formed by etch of the VES metal layer (metal 1) during via hard mask removal using wet

chemical etch. To confirm this hypothesis, another test was run to purposely increase the thickness of metal 1 in VES, and at the same time to reduce the thickness of metal 2 (which is inert to the wet chemical), so that the overall VES thickness remains about the same.

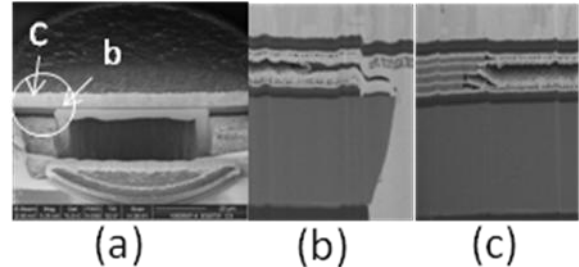


Fig 3 Cross section of via of wafer in group A with increased metal 1 thickness. (a) The overall via shape at the bottom of via, (b) and (c) are amplified view of the via at two locations circled in (a), near a corner of the via (b) and further away from the via (c), respectively.

As shown in FIG 3, via with this modified VES stack is more severely attached than the one shown in FIG 2. (Via in FIG 3 to FIG 5 are flipped upside down relative to FIGs 1-2). Again, this is likely due to the wet chemical etch during the metal hard mask removal. These results indicate that the metal hard mask removal process using wet chemical is not adequate to be used in the overall device fabrication process flow. An improved metal hard mask removal process or alternate integration method is needed.

We then tested a modified via integration method: First, only the SiC was etched, followed by wet chemical removal of the metal hard mask before the GaN etch is performed (group B). It is hoped that the GaN will protect the VES during the hard mask removal process using this method. Results show this is exactly what happened; the VES is not affected at all. However, in many instances, a notching effect was observed at the bottom of the via, as shown in FIG 4 below.

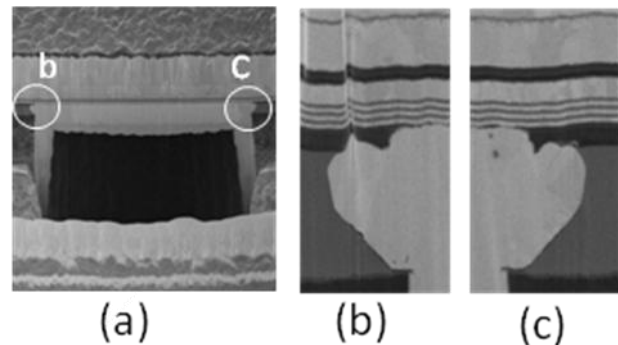


Fig 4 Cross section of via of a wafer in group B. (a) The overall via shape at the bottom of via, (b) and (c) are magnified view of corners of the via shown in (a).

The notching effect was likely caused by the charging of SiC surface due to the absence of the metal hard mask (after the hard mask removal); similar to what has been analyzed previously on etching other materials [16]. The slight notching effect at the bottom of via may not be an issue, as the bottom of via and via side wall still appear to be very well filled with metal during subsequent metallization process. Nevertheless, it is preferred to eliminate such notching to avoid potential void formation during subsequent backside metallization. To this end we explored another integration method, in which the via etching process and sequence are the same as in group A: both SiC and GaN were etched before metal hard mask is removed. However, the final metal hard mask removal process is changed to eliminate the use of wet chemicals that would attack the VES metals. Using this method, the notching effect during GaN etch as observed in group B is avoided. And at the same time, the VES layer is not affected by subsequent metal hard mask removal process as occurred in Group A. Nearly perfect via shape was obtained consistently, as shown in FIG 5.

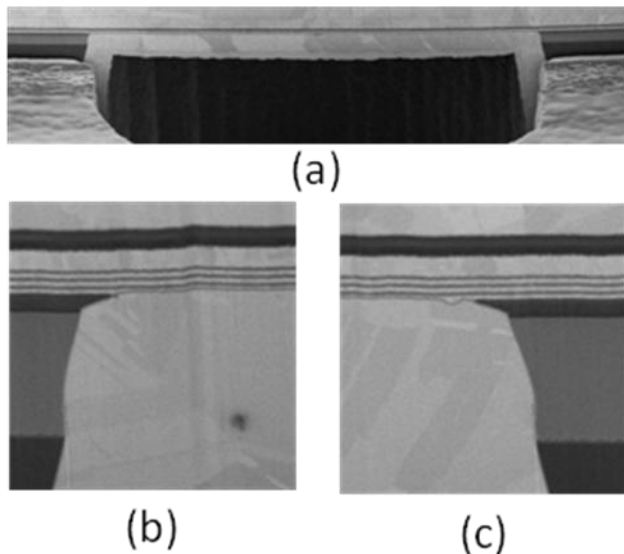


Fig 5 Cross-section of via in group C. (a) The overall via shape at the bottom of via, (b) and (c) are amplified view of corners of the via shown in (a).

CONCLUSION

Wet chemical etching, which is often used for metal hard mask (for via etch) removal can attack the metal in via etch stop (VES) layer under the via. Thus, a hard mask removal process using such wet chemicals presents a potential via and device reliability issue and needs to be sustainably improved. Removing the hard mask before GaN etch can maintain good integrity of the VES layer, but the via shape is degraded due to electric charge build up on SiC surface in the absence of metal hard mask. An alternate metal hard mask removal method that does not involve the use of wet chemicals that could attack VES was established and tested. This new method does not require the modification of the via etch

sequence. Good via profile is maintained with excellent VES integrity obtained consistently.

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ACRONYMS

ICP: Inductively coupled Plasma

VES: Via etch stop