Improving Front Side Process Uniformity by Back-Side Metallization

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Abstract

Plasma processes are an integral and important part of semiconductor device fabrication. The applications include the dry etching of metals, dielectrics, and semiconductors; chemical vapor deposition of thin films and oxygen plasma descum for organics removal. While each of these processes plays a critical role in the performance of the device, process uniformity across the wafer is crucial for consistent probe yield. If the plasma-process condition varies drastically from the center of the wafer to the edge, device performance will change and probe yield will be affected. The critical parameters in a plasma process include temperature, gas flow, gas chemistries, pressure, and effective power. Each of these parameters modifies the etching or deposition-process characteristics. This paper demonstrates that overall process uniformity can be enhanced by metalizing the backside of the wafer. GaAs devices are fabricated on semi-insulating substrates with a bulk resistivity on the order of 1E8Ω-cm. The high resistivity of the substrate inhibits efficient coupling of RF power. This phenomenon is more pronounced at the front end of the wafer fabrication process where the metalized area is usually small.

Introduction

A uniform wafer map with perfect yield is the ultimate goal of every semiconductor fabrication facility. However, this is rarely the case in reality. Quite often, the wafer map would display a distinctive pattern that is caused by one or more process. The micro-loading effect in a plasma-etch process has been studied and is known to cause local etch non-uniformity [1]. A topic that has not been widely discussed is plasma-process uniformity on a macro scale. This paper examines the effect of RF power coupling on plasma-process uniformity.

In a capacitively coupled plasma reactor with a parallel-plate configuration, RF power is applied to one of the electrodes while the other electrode is electrically grounded. Figure 1 depicts a typical parallel plate reactive ion etch (RIE) system.

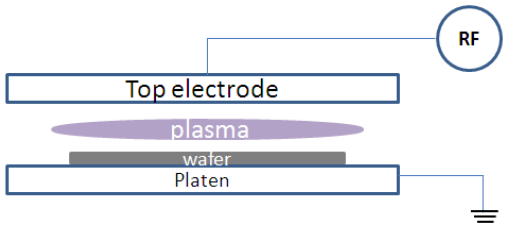

Figure 1 A typical parallel plate RIE system.

GaAs devices are built on a semi-insulating substrate with a bulk resistivity on the order of 1E8 Ohm-cm. The high resistivity that is necessary for integrated circuit (IC) operation will also impede RF-power coupling. This can theoretically lead to non-uniform etching or deposition.

Experiment

To study how RF power coupling may affect the uniformity of our processes, we carried out a series of experiments. Four Gallium Arsenide mechanical wafers were used for each group of experiments. Two of the wafers were sputtered with 1kA of Tungsten Titanium (W-Ti) on the back. The wafers were placed on a special jig so that the front surface did not come into contact with the platen of the sputtering system. All wafers received production 7kA compressive silicon nitride film in a Novellus PECVD tool. The nitride thickness was measured on a Nanospec 6100 reflectometer using a 25 point map recipe with 12mm edge exclusion.

The wafers were put through a short nitride etch in a RIE tool. Standard etch chemistry with SF_6 being the main etch gas was used for the experiment. The etch recipe was created to remove about 2500A of nitride so that there was enough silicon nitride remaining on the wafer for

mapping. The nitride thickness was measured again for thickness using the same 25-point recipe.

RESULTS

After nitride etch, the two groups of wafer looked markedly different. See Figure 2. The back-metalized wafer had a uniform purple color across the entire surface. The wafer without back metal had a green color band about 14mm wide on the edge and a thinner purple ring inside of the green band. A magenta stripe about 50mm wide extended down the middle of the wafer.

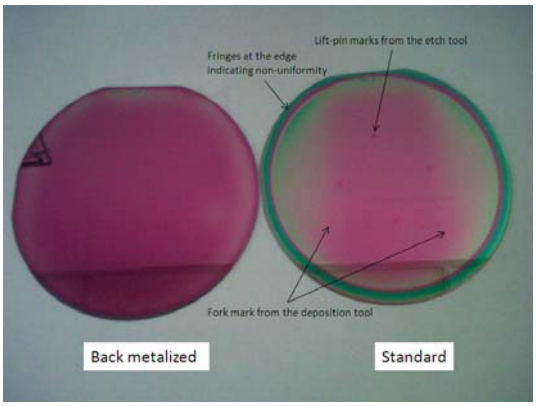

Figure 2 Comparison of back-metalized wafer and standard wafer after nitride etch

Figure 3 shows the wafer platen of the Novellus PECVD system with the fork shaped wafer handler. The magenta stripe fit between the two prongs of the fork and was the imprint of the wafer handler.

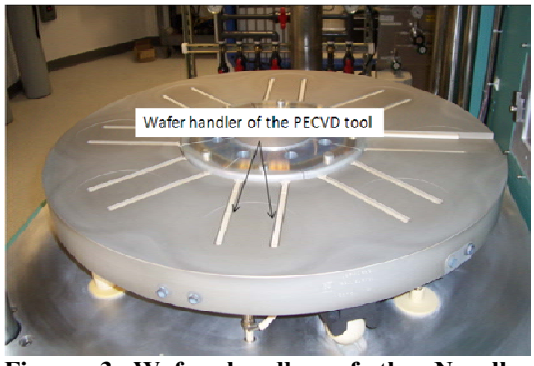

Figure 3 Wafer handler of the Novellus PECVD tool.

The silicon nitride outside of the fork transitioned to a pale green color. Reflectometry measurement indicated that the silicon nitride in this region was 200A to 500A thinner compared to the center of the wafer.

The center of the standard wafer had four 3mm diameter dots at the lift-pins locations on the chuck. The pattern of the RIE chuck (see Figure 4) transferred to the front side of the wafer due to the 200A difference in nitride thickness. The dots measured 4565A compared to 4362A of the neighboring area outside of the fork.

Four holes are machined in the chuck into which the lift-pins retract during processing. The holes cause a change in capacitance and lessen RF power coupling. Lower etch rate therefore resulted on the front of the wafer in the corresponding locations.

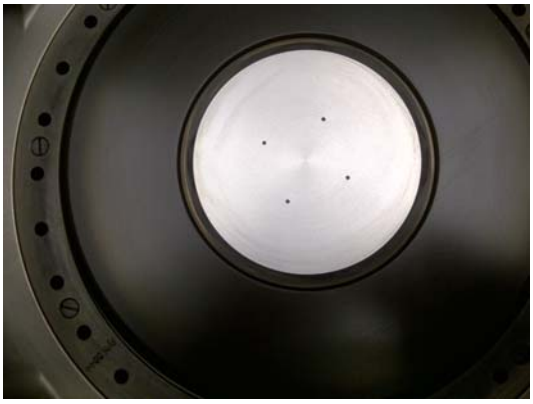

Figure 4 Wafer chuck of the etch tool with the four lift-pins.

Results of the experiment are summarized in table 1.

Table 1 Summary of nitride thickness before and after etch

	Standard wafer	Metalized wafer
Deposited Nitride thickness (Means)	7041A	7112A
Deposited Nitride thickness (Sigma)	67A	22A
Etched thickness (Mean)	4525A	4750A
Etched thickness (Sigma)	121A	27A

The back-metalized wafer had slightly higher deposited nitride thickness. Repeating the experiment confirmed that the difference, although small, is consistent. Without back metallization, the standard wafer had high non-uniformity after nitride deposition. The standard

deviation of the control wafer is 3 times higher than the back-metalized wafer.

After nitride etch, the uniformity disparity grew larger and the fork mark left by the wafer handler became more obvious. The standard deviation for the control and back-metalized wafer are 121A and 27A respectively. The nitride thickness variation of the standard wafers is higher than the data had shown because of the 12mm edge exclusion used in the thickness mapping program.

When blank GaAs wafers were used in the experiment, the results clearly indicated that back-side metallization improved front-side PECVD and plasma-etch uniformity. To determine whether we will realize a measurable yield gain due to the improved uniformity requires running a split lot on actual products. We selected a pHEMT mask where a certain RF parameter is sensitive to a critical dimension in the transistor structure. The critical dimension is controlled by a dry-etch process in a RIE tool. Two of the wafers received 1kA of W-Ti on the back of the wafer. All wafers were randomized and then processed together.

Figure 5 showed the wafer maps of the split lot. The parameter that we seek to improve showed a definite improvement. The two back metalized wafers had 10 percent higher probe yield and the most uniform wafer maps. Comparing the two types of wafers, the improved yield is attributed to the better CD control of the etched pattern. The cross-wafer uniformity of the critical parameter has been successfully improved with the W-Ti back metal. Under-etched and over-etched regions were effectively eliminated improving yield.

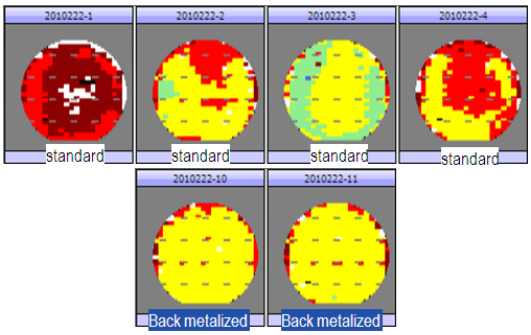

Figure 5 Back-metalized wafers (10, 11) have much more uniform wafer maps than standard wafers (1 through 4).

THEORY

Manual measurement of the silicon nitride film showed an interesting thickness distribution pattern. The nitride at the edge of the wafer in the green band has a thickness of 5696A; about 1400A thicker compared to the area outside of the fork mark. The result suggests that for a bare GaAs wafer with high bulk resistivity, the RF power coupling is weak at the edge. Consequently, the etch rate in a RIE system is generally low in the 12mm band at the edge of the wafer. Any cavity in the wafer chuck such as lift-pin holes or wafer-handler recess in the platen can alter the capacitive and RF power coupling effectiveness and affect the etch and deposition rates. In a semiconductor device where critical dimension is crucial for device performance, this amount of variation will cause performance difference and yield loss. For example, if there is insufficient over-etch built-in in the etch recipe, areas with very low etch rates would have a smaller CD and run a risk of incomplete etch. At the same time, areas with high etch rates may experience enlarged CD and even surface damage.

CONCLUSION

This work demonstrated that plasma process uniformity in a capacitively coupled plasma reactor with a parallel plate configuration has intrinsically poor uniformity for a GaAs wafer. The high resistivity of the semi-insulating substrate inhibits efficient RF power coupling.

A smooth uninterrupted wafer chuck would be best for process uniformity consideration. However, such a design is not possible as the wafer needs to be picked up from the back side. A wafer chuck therefore requires machining to incorporate robots so that the wafer can be handled. The cavities that are necessary to accommodate these mechanical features disrupt the capacitive and RF power coupling. For that reason, the wafer map retains the wafer-chuck pattern. This phenomenon is more pronounced in the front end of the process where metallization area is small. Plasma processes towards the back end of the production flow will be less sensitive due to the larger front side metallization area.

We have repeated the experiment with different dielectrics and polymer films and the results are generally the same. Without back metallization,

the standard wafers have high non-uniformity after plasma etch.

A conductive metal coating on the back of the GaAs wafer greatly improves both the nitride deposition and plasma-etch uniformity. Imprint from the wafer handler and the color bands on the edge of the wafer that are normally present are completely eliminated. The improved uniformity translated into yield gains on masks that are sensitive to CD variation in our HEMT structure.

We plan to continue this work and study if other tool configurations such as a high density inductively coupled plasma (ICP) etch tool and an electro-static chuck will respond similarly to back metallization. In addition, more work is planned to study the effects of back metallization on film growth in a PECVD reactor.

Back metalizing the wafer is a practical solution to yield issues caused by the non-uniformity nature of a GaAs wafer in a capacitively coupled plasma reactor. The 1KA of W-Ti does not clog the grinding wheel and therefore can be implemented into the production flow without issues. The W-Ti film can be etched off in 70ºC H_2O_2, if desired, after the wafer has been mounted on a carrier and before the grind operation.

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