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GaN-on-SiC MMIC Production for S-Band and EW-Band Applications

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An overview and current results of Cree's Title III production capacity program for GaN-on-SiC MMIC on 100-mm-diameter substrates will be presented. This program is focused on Manufacturing Readiness Assessments (MRA) of key metrics including reliability (median (t50%), and 1%-ile lifetime (t1%)), yield, cost, and cycle time. The final program requirement is a Manufacturing Readiness Level (MRL) of eight (8) or higher. The 3-year program is organized into three main phases: baseline assessment, process improvement and final assessment. About half completed, this program is currently in the process-improvement phase. The program has two main MMIC demonstrators: a 75 W S-Band and a 25 W EW-Band die. The die are fabricated with our G28V3 (0.4-µm gate length, 28-V drain voltage) and G28V4 (0.25-µm gate length, 28-V drain voltage) GaN HEMT processes for the S-Band and EW-Band die, respectively. One main goal of the program is to provide an open MMIC foundry for various designers in the industry to take advantage of the benefits of GaN technology.

The Cree GaN HEMT MMIC technology is built on III-nitride epitaxial layers grown by in-house MOCVD on 100-mm diameter, 4-mil thick, high-purity-semi-insulating (HPSI) 4H-SiC substrates. HPSI 4H-SiC substrate manufacturing and GaN HEMT epitaxial growth, being already well-established commercial products, have not been items of focus so far on the program. Insulating GaN with AlN and AlGaN cap layers yields HEMT structures with a channel sheet resistance centered at 335 Ω/□. The defining features of the V3 and V4 technologies include a Ni/Pt/Au gate electrode that is formed by straddling a dielectrically-defined (DD) opening in the first SiN passivation to the AlGaN surface. The 0.4-µm V3 gate length is achieved with standard optical lithography and SiN etch, while the 0.25-µm V4 gate length is achieved using an optical lithography and a standard sidewall spacer. Source-connected field plates are used for improving gain and RF power density, reducing peak fields in the device and thereby improving reliability, and lowering feedback capacitance. GaN MMICs utilize microstrip lines with standard passive components such as dielectrically-supported bridge metal, MIM capacitors, thin film resistors and through-wafer slot vias. The MIM capacitors support peak voltages over 100 V, and the SiC substrate slot vias are implemented in the 4-mil SiC substrates to simplify the layout and increase gain.

The program has completed the baseline assessment and a number of significant process improvement projects. The baseline assessment produced metrics for yield, cycle time and cost. Figure 1 shows that the normalized targets (lines) and actual yields (stars) are on or above plan for the S-Band and EW-Band MMIC die. The yields were improved through quality-improvement tasks to reduce – (1) dc yield detractors like pinched gates; (2) visual yield detractors like channel defects; and (3) line yield detractors like mis-process. Also shown in Figure 1, the die processing cycle time and cost are ahead of plan. Projected die cost reductions are being driven mainly by higher yields, as well as process streamlining and concomitant cycle time reductions. Different projects used to drive improvements to the KPP parameters will be discussed during the presentation.

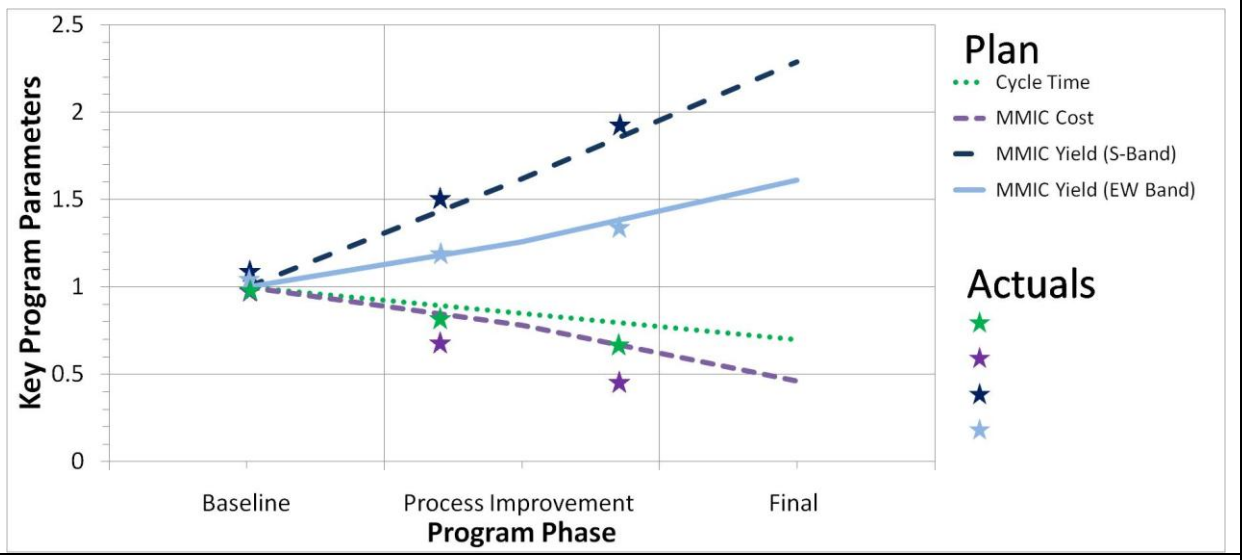

Figure 1 – Key Program Parameters of yield, cycle time and die cost normalized to program start. The lines are the program plan goals, and the stars are actual values to date. As can be seen, the yield is at or above the plan while the cost and cycle time are exceeding program goals.

Cree has performed a thorough MRA that takes into account all aspects of manufacturing, design, technology, quality and reliability by using the Air Force Research Laboratory MRL tool. Specific to this program was inclusion of the yield KPP and the 1% time to fail projections. Figure 2 shows the intrinsic reliability data and lifetime projections for t50% and t1%, for the G28V3 and G28V4 processes. The results show that the intrinsic reliability performance meets and exceeds the program requirements of t50% > 1E6 hours and t1% > 1E5 hours of continuous operation at 125 °C at the back of the MMIC die, which equates to a junction temperature of 225 °C or less for normal operating conditions of the target applications. Both V3 and V4 technologies also passed with zero failures the 1000-h standard qualification tests of high-temperature operating life (HTOL) (28 V, T_j = 225 °C, and 4 W/mm) and high-temperature-reverse-bias (HTRB) (84 V, T_b = 150 °C, and V_G= -8 V). This result demonstrates the voltage robustness of this technology, which has not been reported for other 0.25-µm GaN HEMT released processes. In Year 1 of the program, the G28V3 manufacturing process was assessed at MRL 8 with a production line capability of Low Rate Initial Production and the G28V4 process was assessed at MRL 7.

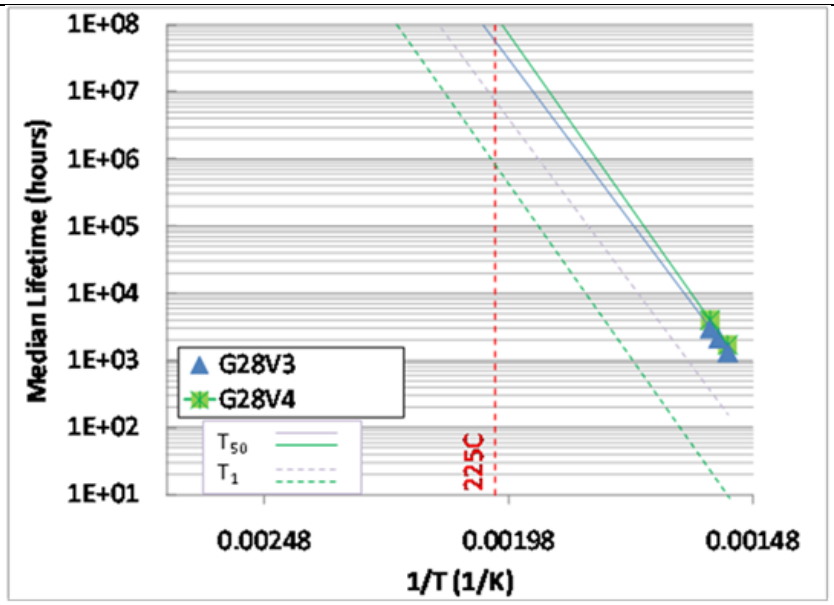

Figure 2 – G28V3 and G28V4 Process Arrhenius results with projections of the mean-time-to-failure (T50, upper solid lines) down to the 1%-tile failure projection (T1, lower dashed lines). The program requirements are fully met on these processes with a T50>1E6 h and T1>1E5 h.