A Study on Al_2O_3 Deposition by Atomic Layer Deposition for III-Nitride Metal-Insulator-Semiconductor Field Effect Transistors

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Al_2O_3 deposited by atomic-layer deposition (ALD) technique is one of the most promising gate dielectrics for MIS devices. Several studies have revealed the impact of ALD deposition recipe and post-deposition annealing recipe to the performance of III-N metal-insulator-semiconductor (MIS) devices [1-3]. While the oxygen sources and annealing conditions have been studied, the impact of process variables and their interactions to electrical properties of MIS high electron mobility transistors (MIS-HEMTs) are still unclear. In this work, we studied six ALD Al_2O_3 deposition and annealing variables using a fractional factorial design of experiments and explored an optimal processing condition to achieve small threshold voltage (V_{th}) shift, low I-V hysteresis and low gate-to-source (GS) diode leakage current for MIS-HEMT processing.

Six experimental factors (n_i) for the ALD deposition and post-deposition annealing recipes were tested in this study using a custom-built ALD tool and Annealsys AS-One annealing system. 15nm-thick Al_2O_3 was deposited on all the samples and annealed in oxygen atmosphere. Each factor has a two-level design, designated as high level (H) and low level (L), respectively. In the designed experiment, the levels of TMA pulse time (n_5) and gas dwell time (n_6) are generated by the other four variables using equations of $n_5 = n_1 \cdot n_2 \cdot n_3$ and $n_6 = n_2 \cdot n_3 \cdot n_4$. This 2^{6-2} fractional factorial design facilitates exploring more factors without increasing the number of samples. The designed n_5 and n_6 provide higher resolution and only high-order interactions are confound in the experiment. The measured responses are V_{th} (at I_D=1mA/mm), I-V hysteresis (ΔV_{th} between forward and reverse sweeps) and GS diode leakage current (defined by $Log_{10}(I_{GS})$ at $V_{GS} = V_{th}$) on circular MIS-HEMT with W_G = 200 μm and $L_{GS} = L_{GD}$ = 1.5 μm. The process conditions applied on each sample and measured responses are shown in Table 1. To better interpret the results, we calculated the effect estimates (E_i) of each variables and interactions. High-order interactions are assumed less effective than main variables and low-order interactions. In Figure 1, the normal probability plot of the effect estimates shows annealing recipe and ALD chamber temperature show strong positive effect while TMA pulse time and gas dwell time have minor negative effect to the V_{th} of MIS-HEMT. This result indicates high anneal temperature, long annealing time and high deposition temperature are preferred for more positive V_{th}. In Figure 2, higher chamber temperature and longer precursor pulse time help reduce the I-V hysteresis of MIS-HEMTs while their interactions (*E35* and *E34*) can increase the hysteresis. This suggests a trade-off exists for the precursor pulse time and deposition temperature. However, considering the results from V_{th}, shorter TMA pulse widths with longer H_2O pulse widths at higher deposition temperature are preferred for lower V_{th} shift and lower I-V hysteresis. In terms of the gate leakage control, higher temperature and longer annealing time shows a trend to reduce the gate leakage while longer precursor pulse width may create leakage path in Al_2O_3 layer, as shown in Figure 3. The interaction of precursor pulse time and chamber temperature (*E245*) indicates that shorter TMA pulse width with longer H_2O pulses at higher ALD growth temperature could lead to an optimal recipe for minimal gate leakage current. Based on this study and the "optimal" growth conditions for the ALD deposition, AlGaN/GaN MIS-HEMTs with L_{GD}=1.5μm showed I-V hysteresis of less than 0.5V, gate-to-source leakage current < 1pA/mm is achieved, and the drain-to-source breakdown voltage >170V, corresponding to lateral breakdown field of 1.1 MV/cm, as shown in the inset of Figure 4.

In summary, we studied Al_2O_3 deposition and annealing on AlGaN/GaN MIS-HEMTs using an ALD deposition technique. A 2^{6-2} two-level fractional factorial design of experiments helps determined an optimal processing to achieve good V_{th} control, low I-V hysteresis, low gate leakage and high breakdown voltage. More details on this study will be discussed in the conference.

Sample number (i)	experimental variables						Responses					
	Gas dwell time [n_6]	TMA pulse time [n_5]	H_2O pulse time [n_4]	ALD chamber temperature [n_3]	Post-dep. anneal Time[n_2]	Post-dep. anneal temperature [n_1]	V_{th} (at I_D=1mA/mm)		ΔV_{th} (between forward and reverse sweep)		Log_{10} (I_{GS}) (at $V_{GS}=V_{th}$)	
							Avg.	Var.	Avg.	Var.	Avg.	Var.
1	L	L	L	L	L	L	-20.6	0.44	1.57	0.003	-7.03	1.78
2	L	H	L	L	L	H	-21.6	0.04	0.33	0.013	-3.96	0.03
3	H	H	L	L	H	L	-22.1	0.21	0.6	0.13	-6.37	0.65
4	H	L	L	L	H	H	-13.3	0.54	1.03	0.003	-13.1	0.02
5	H	H	L	H	L	L	-20.8	0.6	0.07	0.003	-5.17	1.27
6	H	L	L	H	L	H	-15.5	0.02	0.6	0.01	-12.3	0.01
7	L	L	L	H	H	L	-13.6	0.14	0.07	0.006	-7.4	2.47
8	L	H	L	H	H	H	-14.3	0.82	0.67	0.013	-13	0.02
9	H	L	H	L	L	L	-20.1	1.01	0.13	0.003	-4.4	0.01
10	H	H	H	L	L	H	-20.7	1.39	0.2	0.03	-6.55	0.05
11	L	H	H	L	H	L	-16.3	0.02	0.1	0.001	-5.8	1.86
12	L	L	H	L	H	H	-12.9	0.07	0.83	0.003	-12.6	0.01
13	L	H	H	H	L	L	-19.1	0.16	0.13	0.023	-6.17	0.38
14	L	L	H	H	L	H	-15.2	0.14	0.1	0.01	-6.53	1.12
15	H	L	H	H	H	L	-22.2	0.5	0.37	0.003	-5.89	0.16
16	H	H	H	H	H	H	-10.6	0.09	0.3	0.001	-6.68	0.11

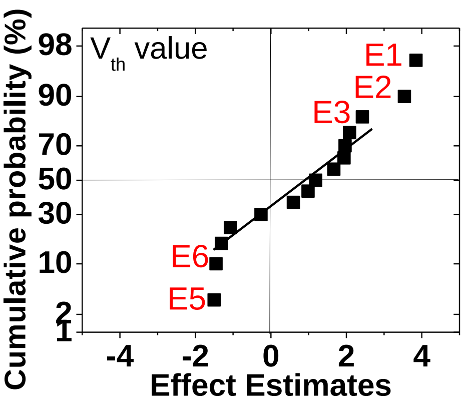

Figure 1 The effect estimates for V_{th} of MISFETs

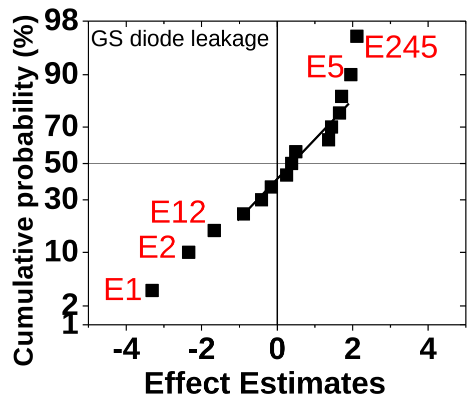

Figure 3 The effect estimates for GS diode leakage current ($Log_{10}(I_{GS})$) at $V_{GS}=V_{th}$.

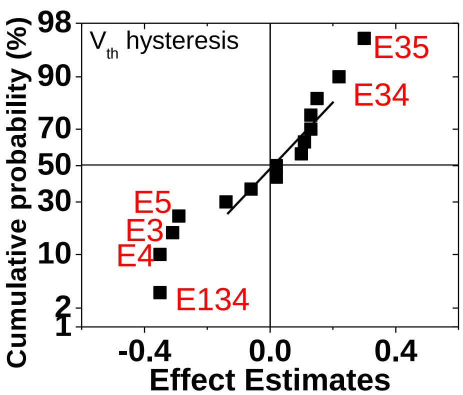

Figure 2 The effect estimates for measured V_{th} hysteresis (ΔV_{th})

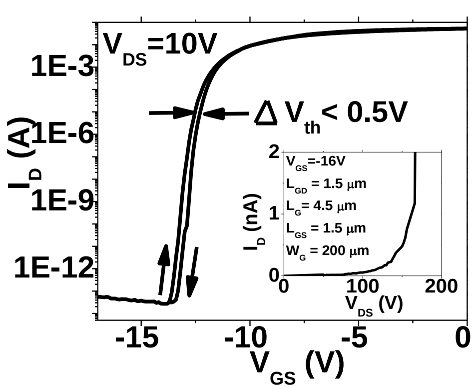

Figure 4 Forward and reverse sweep of transfer curves and breakdown voltage (inset) of MIS-HEMT with W_G = 200µm and L_{GD}=1.5µm.

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