Performance and Reliability of GaN MISHEMTs and MMICs Fabricated From GaN Grown on High Resistance <111> Si Substrates By Molecular Beam Epitaxy

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ABSTRACT

Raytheon has developed state of the art GaN on <111> Si HEMT technology employing molecular beam epitaxy (MBE). The lower growth temperature (~750^{o}C) of molecular beam epitaxy (MBE) relative to MOCVD (~1000^{o}C) results in both improved thermal performance and reduced microwave loss from the III-V/Si interface. These factors combine to enable state of the art, efficient, high power (> 4 W/mm) operation at high frequencies (≥ 10 GHz) that are not usually associated with GaN HEMTs on Si.

The lower temperature MBE growth process reduces the GaN tensile strain upon post growth cool-down which in turn enables a thin AlN nucleation layer to be used in GaN HEMT growth. This stands in contrast to the complex AlGaN/AlN strain compensating layers used in MOCVD based growth that have been shown to significantly degrade the overall thermal conductivity of the III-V epitaxial layers. Additionally, the low temperature MBE AlN nucleation layers result in reduced interfacial charge at the Si/III-Nitride interface. This greatly reduced charge has enabled Raytheon to achieve record low microwave loss (for GaN on Si) of < 0.2dB/mm up to 35 GHz, comparable to GaN on SiC [1].

Most significantly, the record low microwave loss was demonstrated while achieving MBE grown GaN HEMT epi layer quality and uniformity on 100mm high resistance (>1,000 ohm-cm) <111> Si comparable to GaN grown by MOCVD on SiC. Sheet resistances as low as 423 Ohms/sq (± 0.8%) and mobilities of ~1,600 cm^2/V-s have been obtained.

To reduce the gate leakage, Raytheon employed ALD deposited Al_2O_3 as a high k gate dielectric to form MISHEMTs. In order to minimize gate leakage without negatively impacting critical RF device characteristics (like Ft, Fmax, Power, and PAE) a charge balance model was used to design Schottky layer thickness in conjunction with the gate dielectric stack. This was done so that the overall gate capacitance, IDSS, IMAX, and V_T were similar to Raytheon's production microwave GaN HEMT process. The coplanar waveguide (CPW) MBE GaN on Si MISHEMT devices and MMICs were fabricated using an existing mask set designed for GaN on SiC MMIC fabrication. The devices and MMICs had 0.25µm gamma gates. The ohmic and gate contacts are Ti/Al/Pt/Au and Ni/Pt/Au, respectively, similar to Raytheon's production GaN process.

As shown in Figure 1, three terminal leakage test sweeps to V_d = 100V (at V_g = -10V) of GaN on Si MISHEMTs with Al_2O_3 gate dielectric reduced drain leakage by 100-1,000X to V_d = ~45V (V_{gd} = ~55V). Additionally, the pulsed IV test results of the MISHEMT GaN on Si devices were comparable to the Schottky gate GaN on Si control wafer.

CW load pull testing of 10 X 125 µm devices at 10 GHz, V_d = 28V, and I_d =100 mA/mm from several MISHEMT wafers with Al_2O_3 gate dielectric and an $Al_{0.25}GaN$ Schottky layer yielded maximum PAE's in the range of 57-59% and good power performance ~4W/mm as shown in Figure 2. More impressive, however, was the large periphery CPW S-Band MMIC that was fabricated using an existing GaN on SiC design. As shown in Figure 3, the output power of the insulated gate MMIC (tested at V_d = 28V, I_d = 150 mA/mm, and 10% duty cycle) fell within the normal range of GaN on SiC MMICs over the band tested.

Shifting the focus to reliability our single stage 0.25µm gate 10 X 125 µm RF reliability MMICs have successfully completed >2,000 hours operational life testing at V_d = 23V, 100% Duty Cycle, 3-4 dBc, 40ºC base plate while dissipating ~4.5 W/mm at 10GHz (as shown in figure 4). This is after the same devices completed >1,500 hours at 18Vd and survived a 7dB compressed pre-screen at V_d = 35V. Thermal characteristics of these devices were measured using a Raytheon-developed high speed variant of an established gate thermometry technique [2]. Temperature response curves from these measurements exhibit excellent agreement with numerical model predictions incorporating thermal properties measured using time domain thermo-reflectance (TDTR) at Stanford [3] (Figure 5) Finally, DC Arrhenius testing is now underway and will be reported.

To our knowledge, this is the first report of SOA performance for 0.25µm gate GaN on Si MISHEMTs with significant total gate peripheries – with results that are similar to production GaN on SiC.

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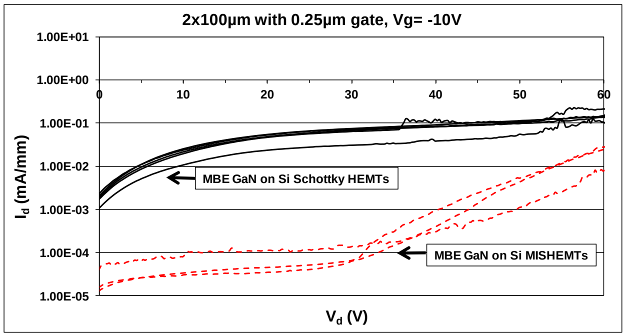

Figure 1. Three terminal leakage plot of I_d vs. V_d swept to Vd=100 with Vgs= -10V for $Al_{0.25}GaN$ MBE GaN on Si MISHEMTs with Al_2O_3 gate dielectric (red dotted lines) compared to 0.25µm 2 X 100 µm 25 nm $Al_{0.25}GaN$ MBE GaN on Si Schottky HEMTs (black solid lines). Each line is a separate device.

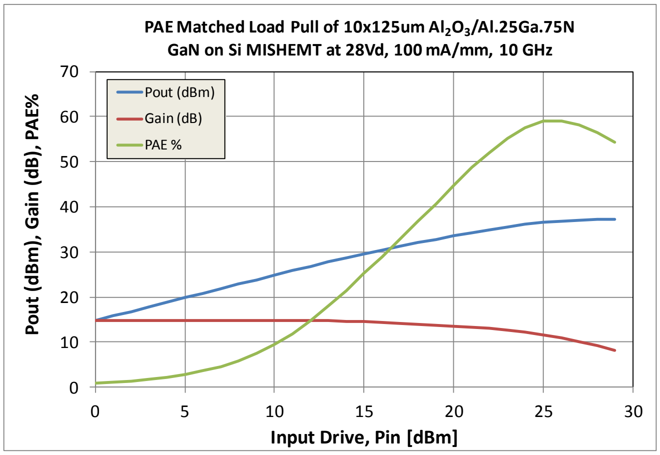

Figure 2. PAE match load pull data at 28 V_d, 100 mA/mm, 10 GHz for a 0.25µm 10 X 125 µm GaN on Si MISHEMT with Al_2O_3 gate dielectric and an $Al_{0.25}GaN$ Schottky layer.

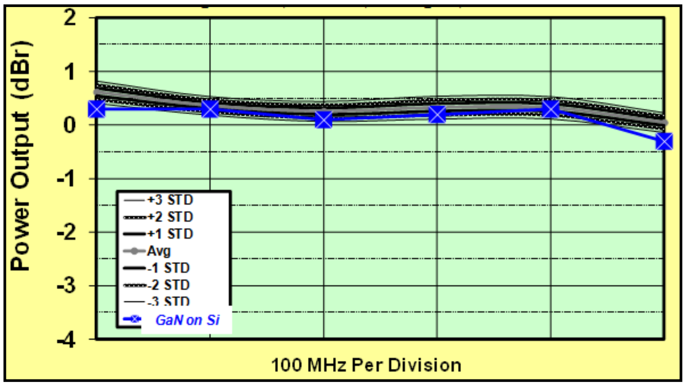

Figure 3. Relative output power (dBr) vs. frequency band of large periphery S-Band MMICs. The 0.25µm insulated gate GaN on Si MMIC (blue line) was fabricated with Al_2O_3 gate dielectric and an $Al_{0.25}GaN$ Schottky layer structure. The 0.25µm Schottky GaN on SiC MMICs (black lines) were fabricated with a slightly thicker $Al_{0.25}GaN$ Schottky than the MISHEMTs.

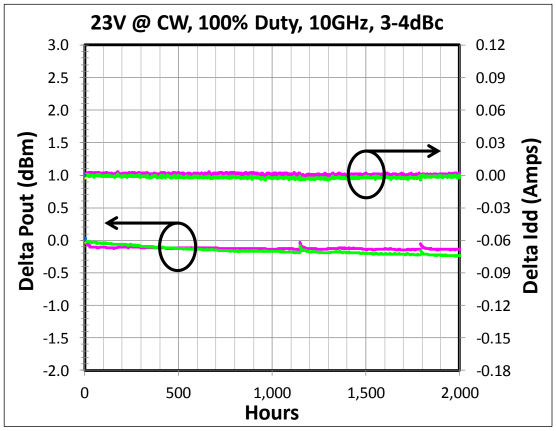

Figure 4. 10 GHz RF operational life test of 0.25µm 10 X 125 µm single stage GaN on Si MISHEMT MMICs at Vd = 23V, 100% Duty Cycle, 3-4 dBc, 40°C baseplate. Pout = ~2.5 W/mm, Pdiss= ~4.5 W/mm.

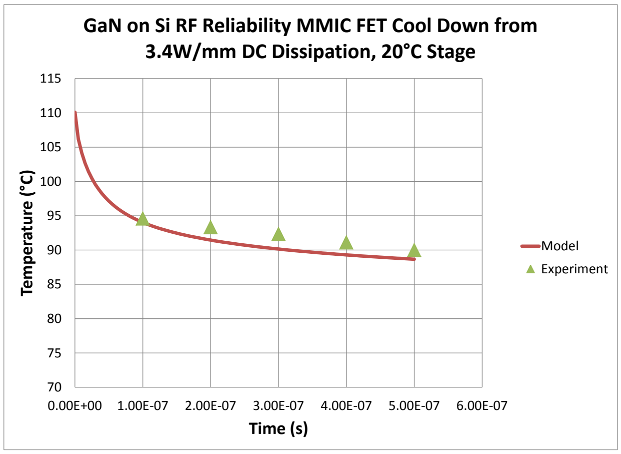

Figure 5. Gate thermometry measured and numerically modeled cooling curve for a 10 x 125 µm single stage RF reliability MMIC