600 V High-Performance AlGaN/GaN HEMTs with AlN/SiN$_x$ Passivation

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Keywords: Current collapse, AlN/SiN$_x$ passivation, OFF-state leakage, high voltage, AlGaN/GaN HEMTs

Abstract

The current collapse suppression capability after high OFF-state drain bias stress of a newly developed passivation technique using an AlN/SiN$_x$ stack structure without multiple field plates in high-voltage AlGaN/GaN HEMTs is demonstrated in this work. The increase of dynamic R_{ON} is suppressed to only 57% of the static R_{ON} during OFF-ON switching after a high drain bias stress of 650 V. The AlN/SiN$_x$-passivated HEMTs deliver a high ON/OFF current ratio of more than eight orders of magnitude. The maximum drain current reaches 900 mA/mm, while the drain leakage current remains below 0.7 μA/mm at V_{DS} up to 600 V with $V_{GS} = -5$ V. Owing to the low OFF-state leakage, a steep subthreshold slope of 63 mV/dec was simultaneously achieved. The breakdown voltage of the AlN/SiN$_x$-passivated HEMTs with a specific ON-resistance of 1.3 mΩ·cm^2 was measured to be 632 V at a drain leakage current of 1 μA/mm, resulting in a high figure of merit (FOM = $BV^2/R_{on,\ sp}$) of 310 MW·cm^2, which is highly desirable for high voltage power switching applications.

INTRODUCTION

GaN-based power devices have been regarded as promising candidates for high-frequency and high-power applications owing to the superior material properties such as high polarization-induced 2DEG density, high electron saturation velocity and high critical breakdown electric field. In spite of these advantages, current collapse has been a major hindrance to the deployment of AlGaN/GaN HEMTs in RF/microwave and power electronics applications [1, 2]. Such techniques as applying SiN$_x$ to reduce surface states in the gate-drain access region and introducing field plates to alleviate electric field strength peak at the drain-side gate edge in the OFF-state were proved to be effective in suppressing this undesired phenomenon [2, 3]. It has been shown that SiN$_x$ passivation needs to be combined with multiple field plates [4] in order to minimize dynamic R_{ON} under high drain bias (V_{DS}) switching. In addition, it still remains challenging to obtain low leakage and low current collapse simultaneously.

Recently, a novel solution that is able to reduce dynamic R_{ON} increase after high OFF-state V_{DS} stress up to 200 V with 4-nm AlN passivation grown by plasma-enhanced ALD was proposed [5]. This approach is simpler and more cost effective compared to the use of multiple field plates since fewer process steps are required. However, the 4-nm AlN is too thin to satisfy the requirements of moisture resistance and the possible implementation of field plate structures in high-voltage AlGaN/GaN HEMTs. Moreover, deposition of thicker films by the ALD technique is impractical due to the slow deposition rate. Therefore, a new passivation structure consisting of an AlN/SiN$_x$ stack, with 4-nm AlN deposited by PEALD and 50-nm SiN$_x$ deposited by PECVD is developed in this work. Both reduced current collapse (or dynamic ON-resistance) and low OFF-state leakage current are achieved simultaneously.

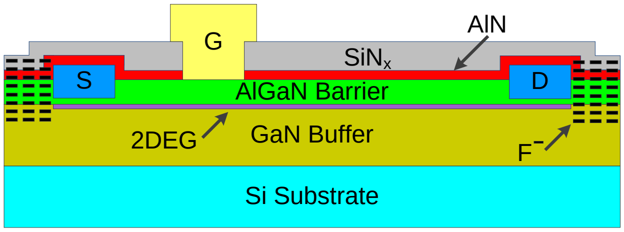

Fig. 1: (a) Cross-section of an AlGaN/GaN HEMT with AlN/SiN$_x$ passivation. The AlGaN/GaN hetero-structure includes a 21-nm AlGaN barrier and a 3.8-μm GaN buffer layer grown on a p-type Si (111) substrate. The T-shape gate features a 1-μm gate footprint and 0.5-μm extension to both sides on top of SiN$_x$.

DEVICE FABRICATION

The AlGaN/GaN-on-Si hetero-structure used in this work consists of a 21-nm AlGaN barrier and a 3.8-μm GaN buffer layer grown on a p-type Si (111) substrate. In Fig. 1, the cross-sectional schematic of the device structure is illustrated. Source/drain ohmic contacts were first formed with Ti/Al/Ni/Au metal stack annealed at 850°C for 30 s in N_2 ambient. Then a 4-nm AlN was deposited by plasma enhanced ALD (PEALD) with *in-situ* remote plasma pretreatment, followed by deposition of 50-nm SiN$_x$ by PECVD. Planar device isolation was then realized by multi-energy fluorine ion implantation. The gate window was opened by ICP-RIE dry etching of the AlN/SiN$_x$ stack layer. At last, the T-shape gate was formed by e-beam evaporation of Ni/Au followed by liftoff.

RESULTS AND DISCUSSION

Device dc electrical characteristics are illustrated in Fig. 2. The AlN/SiN$_x$-passivated HEMTs with a gate-drain spacing of 15 μm deliver an ON/OFF current ratio higher than 10^8 and a steep subthreshold slope of 63 mV/dec with V_{DS} fixed at 5 V, indicating excellent gate control of the 2DEG channel. The threshold voltage V_{th} is extracted to be

−3.2 V (@ I_{DS} = 1 μA/mm). The maximum drain current reaches 900 mA/mm, while the OFF-state drain leakage is below 2 nA/mm at $V_{DS} = 5$ V and $V_{GS} = -5$ V. The OFF-state breakdown behavior of an AlN/SiN$_x$-passivated HEMT with a specific ON-resistance of 1.3 mΩ·cm^2 is shown in Fig. 3. The device was biased at $V_{GS} = -5$ V and the substrate was grounded during the measurement. A breakdown voltage of 632 V is achieved at a drain leakage current of 1 μA/mm, which leads to a high figure of merit (FOM = $BV^2/R_{on,\,sp}$) of 310 MW·cm^2.

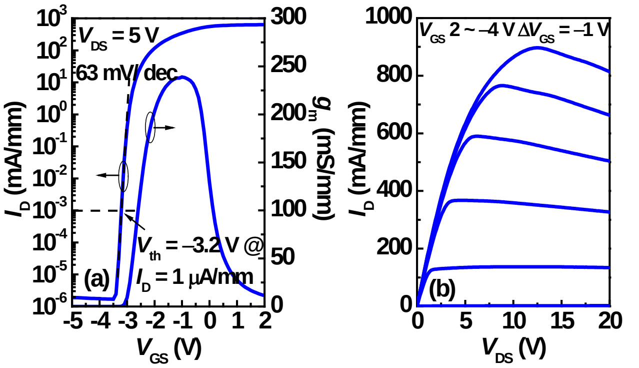

Fig. 2: dc *I-V* characteristics of an AlN/SiN$_x$-passivated HEMT with a gate-drain spacing of 15 μm. (a) Transfer curves measured with V_{DS} fixed at 5 V and V_{GS} sweeping from 2 V to –5 V. (b) Output curves measured with V_{GS} stepped from 2 V to –4 V in steps of –1 V.

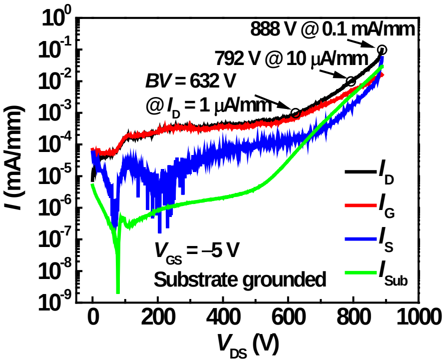

Fig. 3: The OFF-state breakdown characteristics with $V_{GS} = -5$ V and the substrate connected to the ground. A breakdown voltage of 632 V is achieved at a drain leakage current of 1 μA/mm at $V_{GS} = -5$ V and $V_{Sub} = 0$ V, for a device with $L_{GD} = 15$ μm and an $R_{on,\,sp}$ of 1.3 mΩ·cm^2.

The on-wafer switching characterization was carried out from various OFF-state V_{DS} stress (up to 650 V) to evaluate the current collapse of the AlN/SiN$_x$-passivated devices. For V_{DS} stress < 200 V, the measurement setup is the same as that in [5], with a switching interval of ~100 ms. For V_{DS} stress > 200 V, a resistor of 100 kΩ is connected in series with the DUT to the drain terminal for the purpose of over-current protection. In the OFF-state, V_{GS} is fixed at −5 V whereas V_{DS} sweeps from 118 V to 650 V. In the ON-state, V_{GS} and V_{DS} are biased at 1 V and 1.2 V, respectively, corresponding to an ON-state current of ~120 mA/mm [Fig. 4(a)]. As shown in Fig. 4(b), though the dynamic R_{ON} increases with higher V_{DS} stress, it is only 1.58X the static R_{ON} at OFF-state V_{DS} stress of 650 V, suggesting effective suppression of current collapse by AlN/SiN$_x$ passivation. The static R_{ON} is extrapolated in the linear region of the I_D-V_{DS} curve with $V_{GS} = 1$ V as reference. The OFF-ON switching interval is determined to be ~2.7 s (limited by the measurement equipment– Agilent B1505A power device analyzer) by monitoring the waveforms of V_{GS} and V_{DS} during the transient *I-V* characterization.

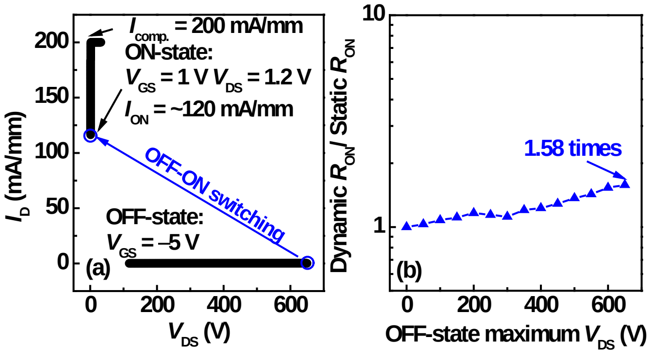

Fig. 4: (a) On-wafer transient switching characteristics of an AlN/SiN$_x$-passivated HEMT with L_{GD} = 15 μm. The substrate was connected to the ground during the measurement. (b) Dynamic R_{ON}/Static R_{ON} with various OFF-state V_{DS} stress from 50 V to 650 V in steps of 50 V. The static R_{ON} is extrapolated in the linear region of the I_D-V_{DS} curve with $V_{GS} = 1$ V as reference.

CONCLUSIONS

A new passivation structure of an AlN/SiN$_x$ stack for high-voltage AlGaN/GaN HEMTs is demonstrated. Current collapse suppression during high voltage transient switching and low OFF-state leakage were realized simultaneously in high-voltage AlN/SiN$_x$-passivated HEMTs without using multiple field plates.

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ACRONYMS

HEMTs: High Electron Mobility Transistors
2DEG: Two-Dimensional Electron Gas
RF: Radio Frequency
PEALD: Plasma-Enhanced Atomic Layer Deposition
PECVD: Plasma-Enhanced Chemical Vapor Deposition
ICP-RIE: Inductively Coupled Plasma Reactive Ion Etching
DUT: Device-Under-Test