Development and Control of a 0.25µm Gate Process Module for AlGaN/GaN HEMT Production

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Abstract

A variety of process modules where developed on 4" GaN on SiC substrates to support a 0.25µm HEMT technology based on i-line photolithographic tools. The technological developments to be discussed pertain to a bi-layer photo-resist shrink on top of Silicon Nitride stress-optimized films; a low-damage inductively-coupled plasma etch, to tailor the dielectric sidewall profile yet tightly control the critical gate foot dimension; a re-patterned metal gate to form a T-gate profile; and the formation of an optimized field-plate structure overtop the T-gate structure. The developmental challenges will be elucidated followed by data showing the stability and control of the critical process modules for high-volume production purposes.

The overview of the process sequence is shown in Fig.1. 0.25µm ODGATE feature is created by first using a single photoresist coating on the initial SiN layer. The ODGATE pattern is transferred from the mask plate to the wafer using a standard, high-volume production i-line stepper and standard 0.25µm lithography technology in WIN. Variability in the CD of the photoresist is found to be caused by Ohmic contact roughness and is correlated to the Drain – Source spacing in the transistor. The Ohmic contacts employed a standard interfacial Titanium layer followed by Aluminum, a barrier layer and a top Gold layer to achieve 0.3 ohm-mm typical contact resistance as shown in Fig.2. A low-damage ICP etch is performed to open the bottom of the T-gate feature in the initial SiN layer without causing significant damage. The schematic cross section of ODGATE profile is shown in Fig.3.

The DRES, gate metal, feature is formed from Nickel-Gold materials using a single layer, negative photoresist lift-off approach as shown in Fig. 4. The field plate structure also is formed using a single layer, negative photoresist lift-off approach. In-line SPC control of ODGATE CD, 1st SiN thickness, and DRES metal CD are shown in Fig.5~7, respectively. The stable in-line control capability could also reflect consistent device cut-off frequency (ft) performance as shown in Fig.8.

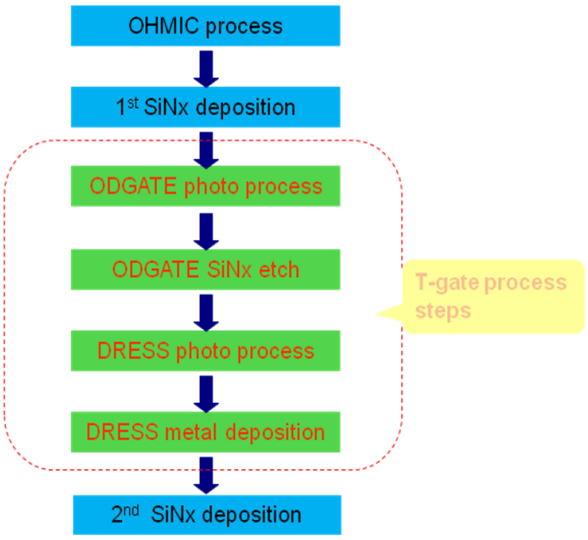

Fig.1 Overview of process sequence for transistor formation

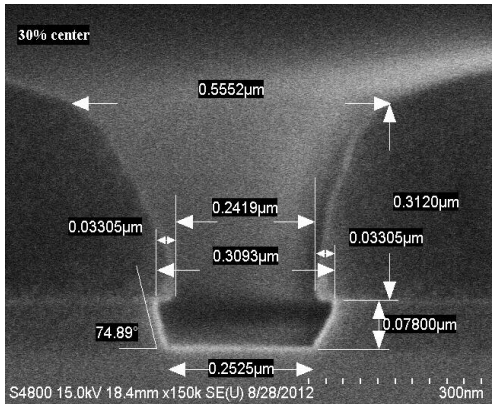

Fig.3 SiN sidewall profile after ODGATE patterning, after ICP etch, and with photoresist still present

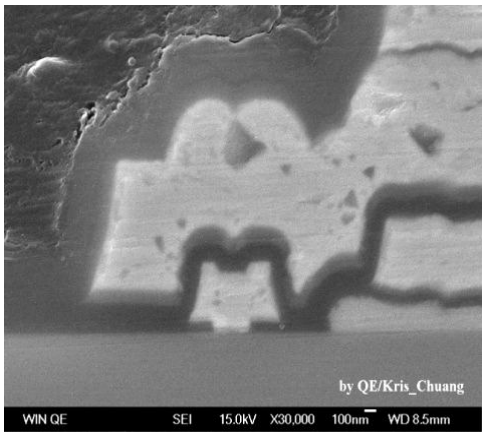

Fig.4 Ohmic, Gate metal and Field-plate profile

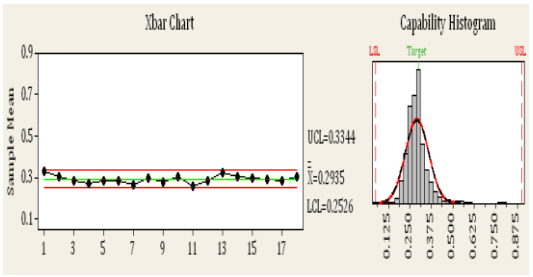

Fig.2 Ohmic contact resistance control data (wafer basis)

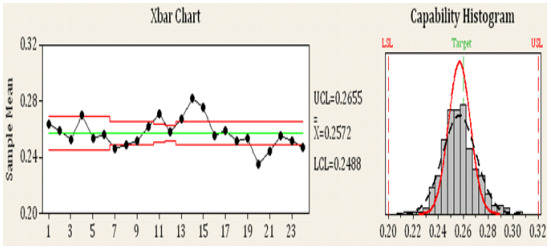

Fig.5 SiN ODGATE CD control after ICP etch measured by CD-SEM (lot basis)

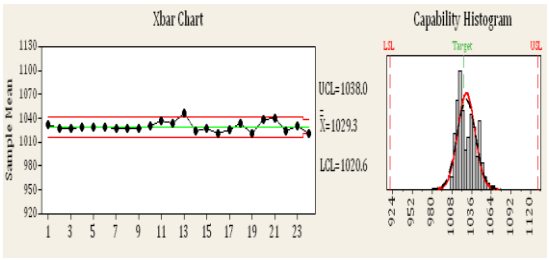

Fig.6 1st SiN thickness control data (lot basis)

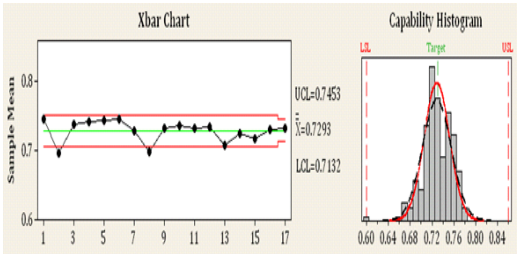

Fig.7 DRES metal CD control measured by CD-SEM (lot basis)

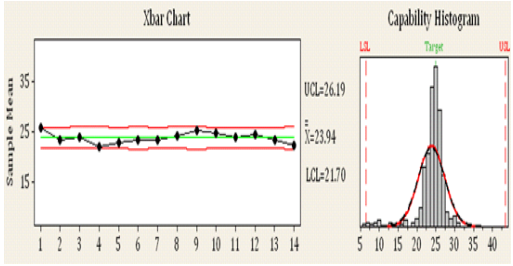

Fig.8 Wafer acceptance test capability of ft (GHz) (wafer basis)