Wafer-level Backside Process Technology for Forming High-density VIAs and Backside Metal Patterning for 50-μm-thick InP Substrate

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Recently, InP-based sub-millimeter-wave monolithic ICs (SMMICs) have attracted much attention because they are key components in broadband wireless communications systems and terahertz imaging systems [1]. For stable operation of SMMICs, a wafer-level backside process for thinning down a substrate and forming ground VIAs is necessary in order to eliminate ground bounce and substrate resonance. Despite the importance of the backside process, its details from the viewpoint of IC operations have not been reported. We present a backside process for thinning 3-inch InP substrates down to 50 μm, forming dense VIAs with good uniformity across the whole substrate, and backside-metal patterning, which is applicable for up to Y-band SMMICs.

We clarified the required thickness of an InP substrate and density of the VIAs. The RF transmission properties of the thinned substrate with VIAs were evaluated with a simple model where the fundamental mode propagates from one end-face to the other of the chip with VIAs. As shown in Fig. 1, distractive transmission, which causes a substrate resonance, can be eliminated when the chip is thinned down to 50 μm and VIAs are formed with an edge-to-edge gap of 50 μm. Our backside process was developed to achieve this geometry. The process begins with thinning down a 3-inch InP substrate after topside IC formation. This is followed by VIA formation, electroplating, wire-patterning, and dicing (Fig. 2). Throughout the process, the InP substrate is adhered upside down to a glass substrate. After the InP substrate has been ground down to 50 μm, HI-based inductively coupled plasma reactive ion etching (ICP-RIE) is performed to form the VIAs. As the halogenated production of the etched InP efficiently sublimates at over 150 ^{o}C [2], we can obtain finely shaped VIAs without residue by keeping the substrate temperature higher than 150 ^{o}C during the RIE. Because the InP etching rate is very sensitive to the temperature, the geometries of the formed VIAs show significant deviation over the whole substrate and in every run if the temperature is not both uniform across the 3-inch substrate and constant during RIE. Furthermore, the temperature should be lower than the degradation temperature (~ 170 ^{o}C) of the adhesive layer. We achieve precise and reproducible control of the substrate temperature by introducing an intermittent cooling step during the RIE. With this etching sequence, we obtain uniform geometry of VIAs with a 20 to 100 μm diameter: Deviation (σ) of VIA diameter is less than 1.8 %, which is small enough to form high-density VIAs with an edge-to-edge gap less than the target 50 μm (Fig. 3). Their tapered shapes broadening toward the backside are preferable for forming a conformal deposition of a metal seed layer for electroplating. After the Au seed layer has been sputtered, selective electroplating is performed with a spray-coated nega-type resist. The use of the nega-type resist avoids under-exposed resist residue inside the VIAs at development of the coated resist, and the spray coating ensures conformal resist coverage inside the VIAs. With these techniques, an Au electroplating layer is formed inside the VIAs without voids (Fig. 4). The Au seed layer is removed by conventional RIE and a backside-patterned chip is obtained. We demonstrate the developed backside process with an on-chip antenna for RF wireless interconnection. The Au seed layer just under the antenna fabricated on the topside is finely removed (Fig. 5). Figure 6 shows the resistivity of VIAs per unit area when the VIAs are formed with the smallest gap, which is determined by 3σ (σ is shown in Fig. 3). With the scaling-down of VIA diameter, the resistivity decreases proportionally. This result shows that scaling-down and minimizing the gap are advantageous for ground stabilization. Although VIAs with a diameter of less than 40 μm show almost the same resistivity, aggressive scaling-down of VIAs has a benefit in flexibility of VIA layout in SMMICs.

In conclusion, we developed wafer-level backside process technology that consists of thinning the substrate to 50 μm, forming dense and uniform VIAs with an edge-to-edge gap of 35 μm, and making fine backside-metal patterns. This technology is promising for fabricating SMMIC chips with stable operation and boosting their operating frequency to 500 GHz.

[1] M. J. Fitch et al., “Terehertz Waves for Communications and Sensing”, *J. Hopkins APL Tech. D.*, (2004), Vol. 25, No. 4, pp.348-355.

[2] R. J. Shul et al., “Temperature Dependent Electron Cyclotron Resonance Etching of InP, GaP, and GaAs”, *J. Vac. Sci. Technol. A*, Vol. 14, No. 3, pp1102-1106, 1996.

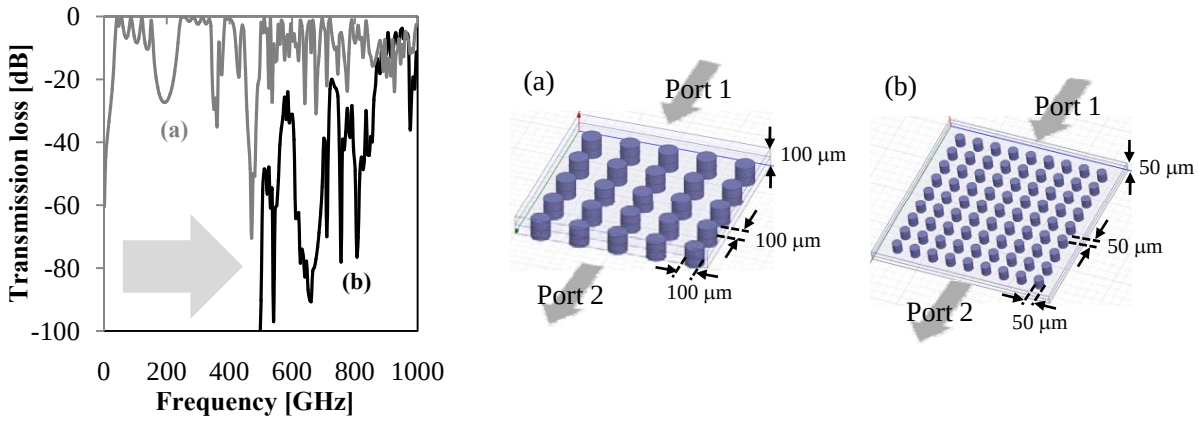
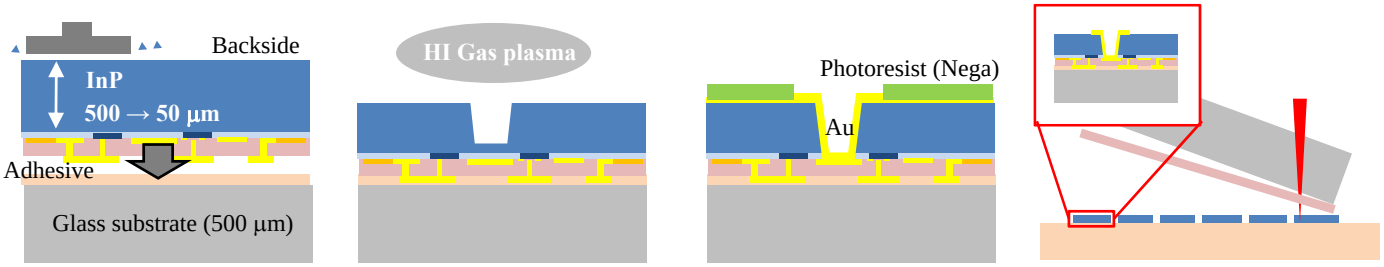


Fig. 1. Simulated fundamental mode transmission of the thinned substrate with VIAs. (a) With a 100-µm-thick substrate and 100-µm-gap VIAs; (b) with a 50-µm-thick substrate and 50-um gap VIAs.



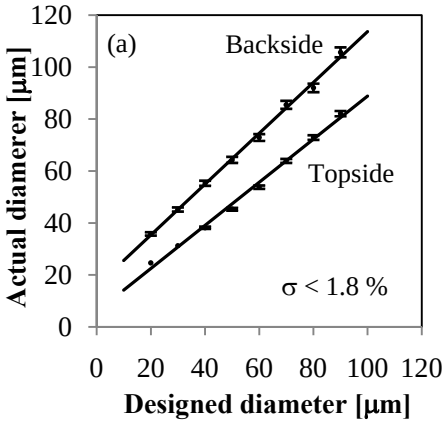
(a) Supporting with glass substrate and thinning

(b) Etching substrate by HI-based ICP-RIE

(c) Patterning with electro-plating and seed-layer etching

(d) Dicing and demounting a supporting glass substrate

Fig. 2. Backside process flow for InP ICs.



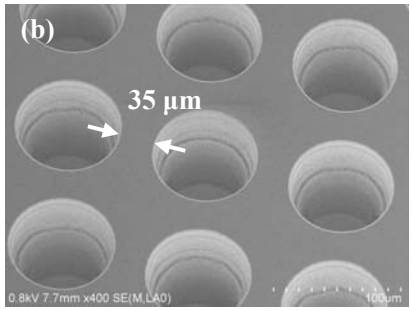


Fig. 3. (a) Uniformity of fabricated VIAs with a 20 to 100 µm diameter. (b) SEM image of the fabricated VIAs with a gap of 35 µm.

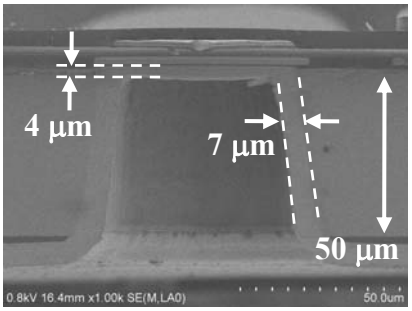


Fig. 4. Cross-sectional SEM image of Au-electroplated VIA.

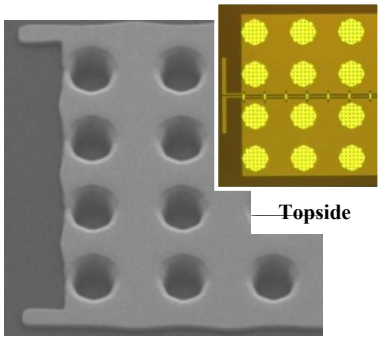


Fig. 5. Backside-patterned on-chip antenna.

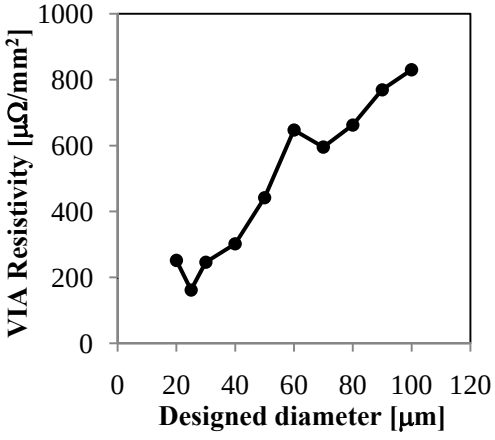


Fig. 6. Dependence of resistivity of closest formed VIAs on VIA diameter.