

## Formation of slanted gate trenches in silicon nitride using thermally reflowed ZEP 520A and $\text{CHF}_3/\text{SF}_6$ plasma etching

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Fabrication of gates is the most crucial part in transistor manufacturing due to its strong influence on device performance and reliability. Currently, the most commonly used technology for GaN-based HEMTs and MMICs is the so-called “embedded gate” process, where gate metal is deposited into the trench opening etched in a dielectric passivation layer (usually silicon nitride,  $\text{SiN}_x$ ). The semiconductor surface properties at the bottom of the trench opening along with the semiconductor/metal interface quality decide on electrical characteristics and reliability of the transistors. Since trench etching of the dielectric layer also affects the semiconductor surface, the etching process of the dielectric needs to be carefully controlled to minimize detrimental effects on the device performance. Moreover, the trench etching should provide a trench geometry that allows for conformal metal coverage without void formation. A trapezoid profile of the gate trench would not only improve homogeneity of metal coverage but also device performance by formation of slant field plates. It has been shown that such integrated slant field plates can reduce dc-RF dispersion and parasitic capacitance in AlGaIn/GaN HEMTs [1]. In this work we present the development of a  $\text{SiN}_x$  etching process using thermally reflowed ZEP 520A electron beam resist as etch mask. The influences of reflow time and temperature on structure size and sidewall angle are studied. The dependencies of  $\text{SiN}_x$  etch rate, RF bias level, and etching selectivity of  $\text{SiN}_x$ /ZEP mask on process parameters are determined. A bulk  $\text{SiN}_x$  etch rate of  $\sim 118$  nm/min at RF bias level of 8 V has been obtained. At these conditions  $\text{SiN}_x$ /mask selectivity is 2.5. A 50 nm wide bottom of the  $\text{SiN}_x$  trench with a sidewall slope of  $77.5^\circ$  has been achieved.

All experiments were performed on 4 inch s.i. GaAs wafers with 100 nm thick  $\text{SiN}_x$  films deposited at  $345^\circ\text{C}$  using a Sentech SI500D PECVD tool. ZEP 520A resist was 50% diluted, spun at 2000 rpm, and baked for 3 min at  $115^\circ\text{C}$  during, resulting in a final thickness of  $\sim 210$  nm. Exposure was performed using a Vistec SB251 electron beam lithography tool with an acceleration voltage of 50 kV and a dose of  $65 \mu\text{C}/\text{cm}^2$ . After development wafers were cut into  $\sim 1 \text{ cm}^2$  square samples. Reflow of the resist was performed on a calibrated hotplate at different temperatures and time intervals. After reflow, samples were etched using Sentech SI500 ICP tool. Size and profile of trench openings in  $\text{SiN}_x$  were analyzed using scanning electron microscopy (SEM).

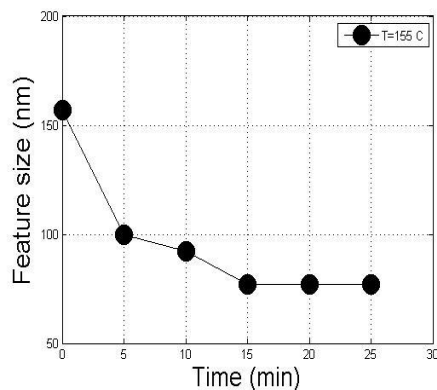


Figure 1. Dependence of feature size on reflow time for a reflow temperature of  $155^\circ\text{C}$ .

For proper mask fabrication by thermal reflow it is essential to obtain sloped sidewalls by profile rounding and to increase plasma stability of the resist [2]. Recently, for 235 nm thick ZEP 520A-7 on silicon (100) an onset of profile rounding at  $145^\circ\text{C}$  was reported [3]. In our experiments no reflow could be observed at temperatures below  $150^\circ\text{C}$ . The difference might be caused by the different degree of resist dilution and thickness or by the substrate material and thickness. Figure 1 shows the dependence of the critical dimensions on the reflow time for a hotplate temperature of  $155^\circ\text{C}$ . As can be seen from the graph, the feature size shrinks mainly within the first 5 minutes, then the reduction slows down and the feature size decreases with a rate of about 2 nm/min, and finally saturates after 15 minutes. In this case the feature size shrank by about 80 nm.

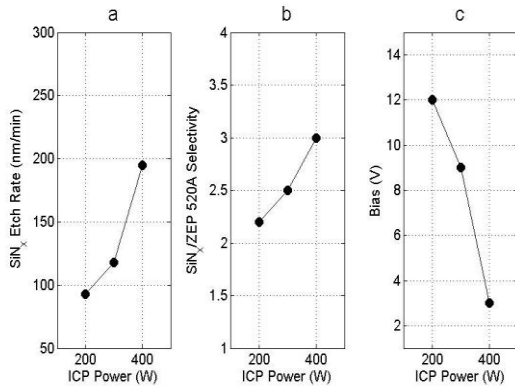


Figure 2. Dependencies of a) SiN<sub>x</sub> etch rate, b) SiN<sub>x</sub>/mask selectivity and c) bias level on ICP power level for a CHF<sub>3</sub>/SF<sub>6</sub> flow ratio of 15.

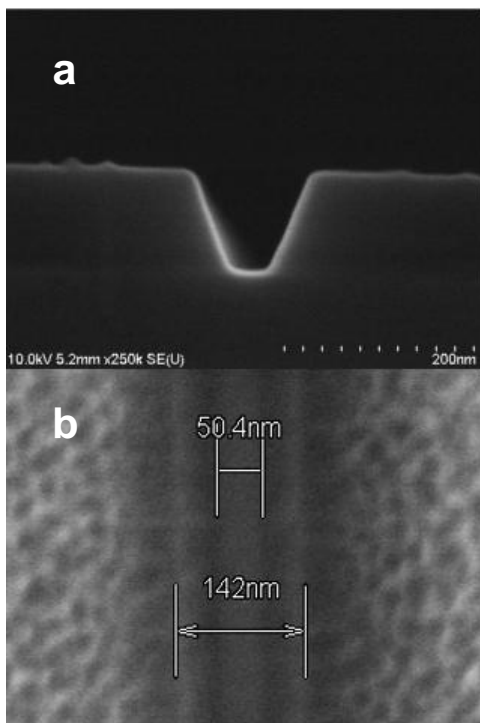


Figure 3. SEM images of a) a cross section and b) a top view of 50 nm slanted SiN<sub>x</sub> trench (top view with resist mask)

This reflow behavior provides a large process window and allows flexible attuning to requirements of plasma etching. A more detailed investigation of the resist behavior at even higher reflow temperatures including an evaluation of the resist profiles will be presented in the extended paper.

Requirements for the dry etch process comprise low bias, high degree of anisotropy and good SiN<sub>x</sub>/mask selectivity. In order to meet this, RF power level and process pressure were fixed at the lower limit of etching tool capabilities, which are 10 W and 2 mTorr, respectively. CHF<sub>3</sub>/SF<sub>6</sub> flow ratio and ICP power level were varied to optimize process conditions.

As shown in Fig. 2 (a), the etch rate of SiN<sub>x</sub> sharply increases with higher ICP power level. At 400 W ICP power the etching of a 100 nm deep trench takes 30 s. This is relatively short and can deteriorate process repeatability. In order to avoid this, it is necessary to reduce the ICP power level. Figs. 2 (b) and (c) show a strong correlation between ICP power level, process selectivity and RF bias. In terms of bias and selectivity it is better to use regimes with higher ICP power, but as shown above there is a limitation by process time. An ICP power level of 300 W allows for a sufficient level of anisotropy of 2.5 and a bias level of 8 V, which satisfies the given requirements. The influence of the CHF<sub>3</sub>/SF<sub>6</sub> flow ratio on anisotropy and other process properties will be detailed in the full paper.

Fig. 3 shows SEM images of a slanted SiN<sub>x</sub> trench obtained with the following parameters: ICP power level 300 W, background pressure 2 mTorr, RF power 10 W and CHF<sub>3</sub>/SF<sub>6</sub> flow ratio 15. The etch rate of SiN<sub>x</sub> for this process was 118 nm/min with a SiN<sub>x</sub>/mask selectivity of 2.5 and a bias level of 8 V. Smooth sidewalls and bottom morphology of the trench along with a well-defined trench opening throughout the full

trench line were obtained. The developed process will be implemented in the process flow of AlGaIn/GaN HEMT and MMIC fabrication for Q-band applications. Electrical data of fabricated transistors along with process yield and reproducibility on 4 inch wafers will be presented in the full paper.

#### References

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