Process Improvements for an Improved Diamond-capped GaN HEMT Device

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Reduced performance in GaN-based high electron mobility transistors as a results of self-heating has been well-documented. Diamond has been proposed as an integrated heat sink layer, either by direct growth of the HEMT structure on diamond substrates or capping of the device with CVD diamond. We have previously reported improved electrical performance and reduced self-heating in a "diamond-before-gate" approach, shown in Figure 1, which improves the thermal budget of the process by depositing NCD before the thermally sensitive Schottky gate and enables large-area diamond [1,2]. These devices have implemented a thin dielectric layer between the HEMT and the NCD cap to passivate the HEMT surface and protect the HEMT from damage in the NCD growth process, which employs high temperature and high density H_2/CH_4 microwave plasma. A significant drawback to this approach is that the passivation layer, however thin, acts as a thermal insulator between the hottest part of the device and the heat spreading layer. In the second generation of devices, we have improved the diamond nucleation and initial growth processes to enable the direct deposition of diamond on the AlGaN/GaN surface, and demonstrated working HEMTs with this process, shown in Figure 2. This is an especially advantageous device structure – not only is the heat spreading layer in direct contact with the heat source, but the reduction in current collapse, shown in Figure 3, indicates that diamond is an adequate passivation layer. In this process, the most critical step is the reliable formation of the gate opening without damaging the now unprotected GaN surface in the diamond etch, which involves a high power plasma etch in O_2-based chemistry. Hall measurements taken at multiple points in the process indicate that while the diamond deposition process does not degrade the HEMT, overetching in the gate opening step results in significantly degraded mobility and carrier density in the region under the gate, as shown in Table I. To mitigate this effect and produce a reliable gate opening, we have developed a sacrificial gate after diamond process, where the gate "recess" is formed as a SiN_X pillar before diamond growth, followed by either a realignment of the gate recess or selective diamond growth outside of the gate region. This approach is expected to improve the yield and scalability of the diamond directly on GaN process.

References

[1] M.J. Tadjer, et. Al. IEEE Electr. Dev. Lett. **33**, 23-25 (2012)
[2] T.J. Anderson, et. Al. Device Research Conference 2012 Proceedings

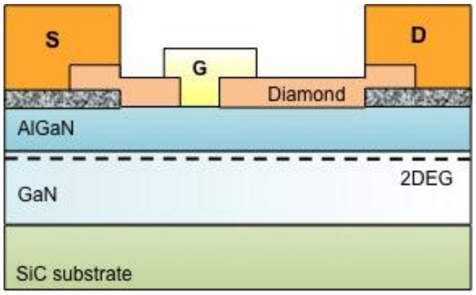

Figure 1. Schematic of “Diamond after Gate” HEMT with diamond directly On GaN

	Hall		
	R_{SH} (Ω/□)	μ (cm²/V-s)	N_{SH} (cm^{-2})
Reference	533	1500	$7.83x10^{12}$
After NCD	553	1390	$8.15x10^{12}$
After Gate Etch	$1.72x10^{6}$	464	$2.04x10^{9}$

Table I. Hall measurements before and after diamond growth and the gate recess opening

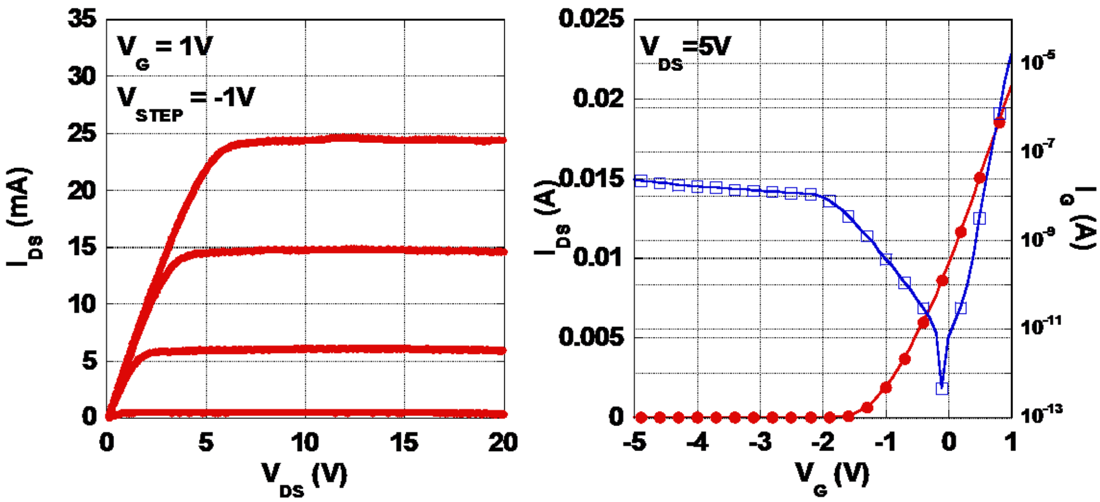

Figure 2. Transfer curves for NCD-capped HEMT with diamond directly on GaN

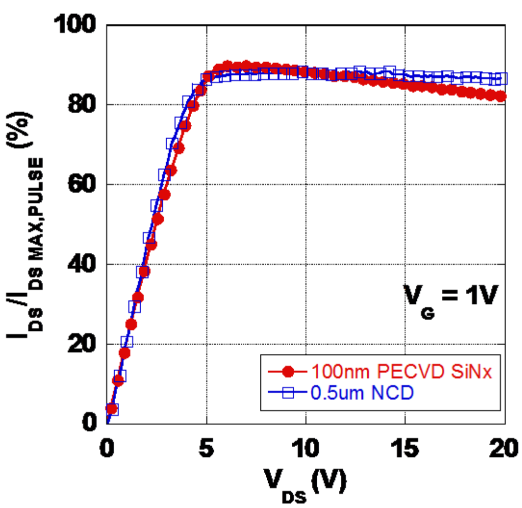

Figure 3. Current collapse in NCD-capped and SiNx-passivated HEMTs under DC operating conditions, quantified by decrease in $I_{DS,MAX}$ relative to pulsed I-V.