Effect of sputtered SiN passivation on current collapse of AlGaN/GaN HEMTs

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GaN-based HEMTs promise high power and high frequency operation due to the material advantages such as high breakdown field, high electron mobility, and high electron saturation velocity. Even though many progresses have been achieved, there still remains some issues especially dynamic on-resistance degradation or current collapse which seriously limits the microwave output power and switching performances. Although significant improvements have been achieved recently by various approaches such as surface passivation [1] and surface charge control with GaN cap layer [2], it is still a fundamental issue to understand the mechanism of the current collapse in detail. In this work, effects of sputtered SiN passivation on current collapse have been studied by monitoring the dynamic change in on-state resistance (R_{ON}). R_{ON} ratio is also measured in terms of post-deposition annealing temperature.

An AlGaN/GaN-based heterojunction was grown by MOVPE on a c-plane 3-inch sapphire substrate. It consists of undoped GaN channel and undoped $Al_{0.25}Ga_{0.75}N$ barrier layers with thicknesses of 1μm and 25nm, respectively. Planar-type HEMT devices were fabricated by evaporating Ti/Al/Mo/Au as ohmic electrodes and Ni/Au as Schottky electrodes. The gate-to-source (L_{gs}), gate length (L_g) and gate-to-drain (L_{gd}) distances were 2, 3, and 10μm, respectively. The gate width was 200μm. Four types of devices were fabricated having passivation layers of SiN with different deposition temperatures, i.e. 100, 150, 200, and 250°C (defined as device A, B, C, and D, respectively) for controlling the surface condition. SiN passivation layer was deposited by sputtering with a thickness of 150nm. The maximum drain currents were almost the same (around I_{DSmax}=380 mA/mm) for the four devices at V_{GS} =1V. For device A, post annealing was performed from 300 to 500°C for 10 min in N_2 flow. The $R_{ON(DC)}$ was measured at constant drain current, I_{DS} =10mA and V_{GS} =1V without stress voltage (V_{stress}). The $R_{ON(pulse)}$ was measured at a constant I_{DS} of 10mA and at V_{GS} =1V, using pulsed conditions with an on-state time (t_{on}) of 1μs and an off-state time (t_{off}) of 1ms. The pulse was applied from off-state (V_{GS} =-5V with V_{stress}) to on-state (V_{GS} =1V with constant I_{DS} =10mA). In order to keep I_{DS} constant, the load resistance (R_L) was varied from 1 to 15kΩ. The R_{ON} ratio is defined as $R_{ON(pulse)}/R_{ON(DC)}$. All the devices were measured at room temperature and in the dark.

Figure 1 shows the deposition temperature dependency of R_{ON} for both $R_{ON(DC)}$ and $R_{ON(pulse)}$ (with V_{stress} =100V). The R_{ON} was decreased with increasing the deposition temperature. The amount of R_{ON} change was larger for pulsed measurement as compare to DC one. Figure 2 shows R_{ON} ratio as a function of deposition temperature with different V_{stress}. The R_{ON} ratio was also decreased with increasing the deposition temperature and became high with increasing V_{stress}. These results suggest that the SiN/AlGaN interface trap density is reduced with the increase in deposition temperature. Figure 3 shows the effect of post-annealing temperature on R_{ON} ratio with different V_{stress} for device A. The R_{ON} ratio was decreased with the increase in annealing temperature (see Fig. 3(a)). The consistent results were observed for higher V_{stress} (see Fig. 3(b)). These results also indicate that the SiN/AlGaN interface trap density is reduced with increasing the post-annealing temperature. Time dependent R_{ON} ratio was measured for device A, as shown in Fig. 4. The R_{ON} ratio was decreased with increasing t_{on} for a fixed t_{off} of 1ms (Fig. 4 (a)), while it was increased with increasing t_{off} for a fixed t_{on} of 1μs (Fig. 4 (b)). More detailed analysis on the time dependence of R_{ON} ratio will be presented at the conference.

[1] B. M. Green, et al., IEEE Electron Device Lett., vol. 21, pp. 268–270, June 2000

[2] T. Kikkawa, et al., in IEDM Tech. Dig., 2001, pp. 585–588.

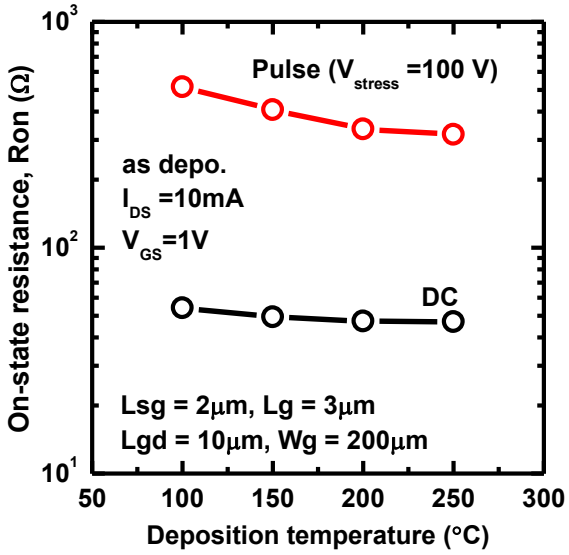


Fig. 1 On-state resistance (R_{ON}) vs deposition temperature.

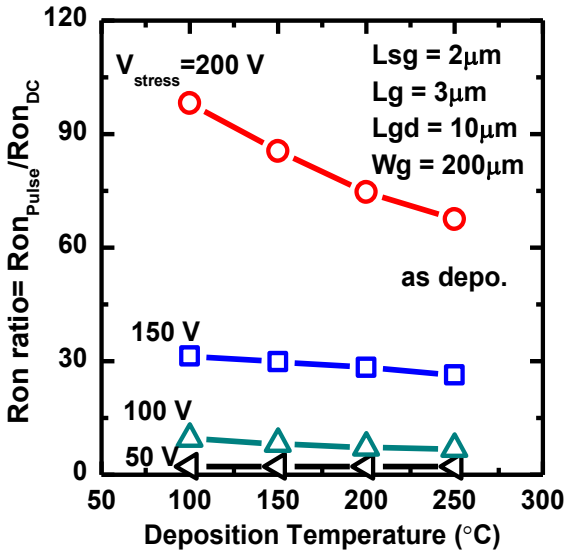
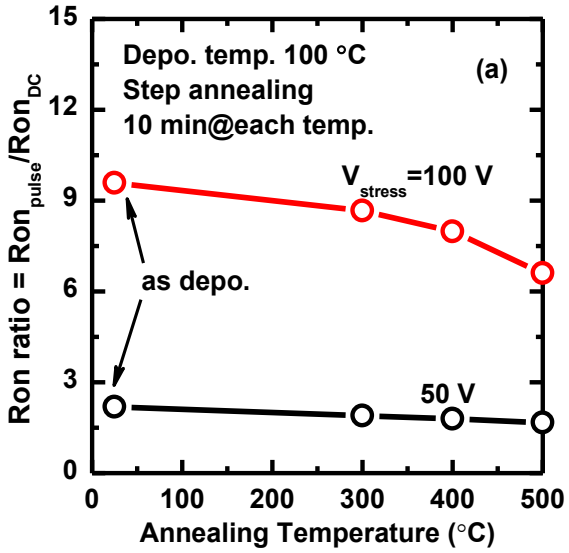


Fig. 2 R_{ON} ratio as a function of deposition temperature.



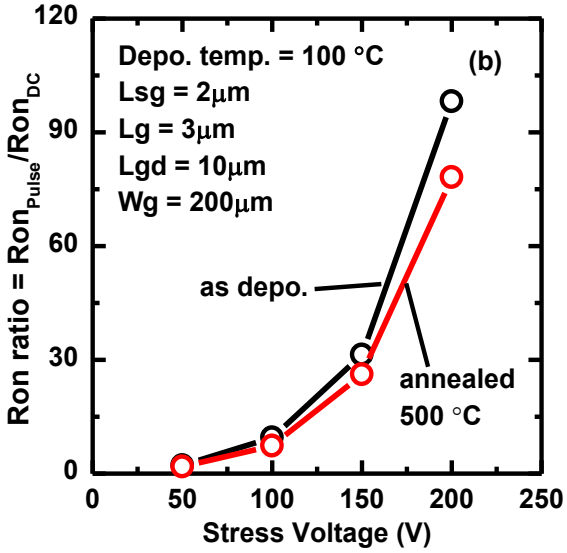
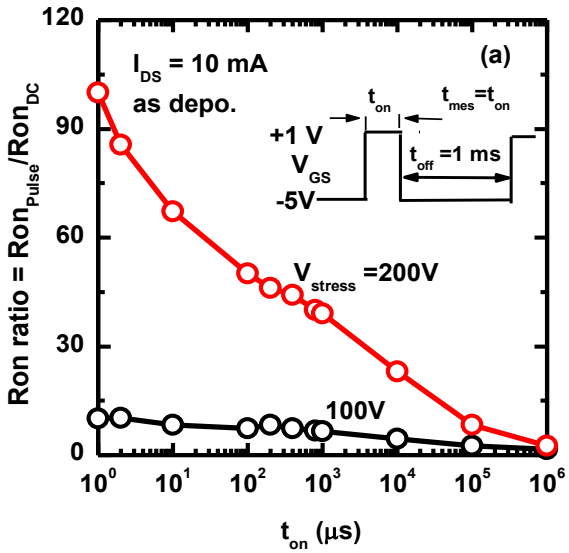


Fig. 3 R_{ON} ratio vs annealing temperature (a) and R_{ON} ratio vs stress voltage (b).



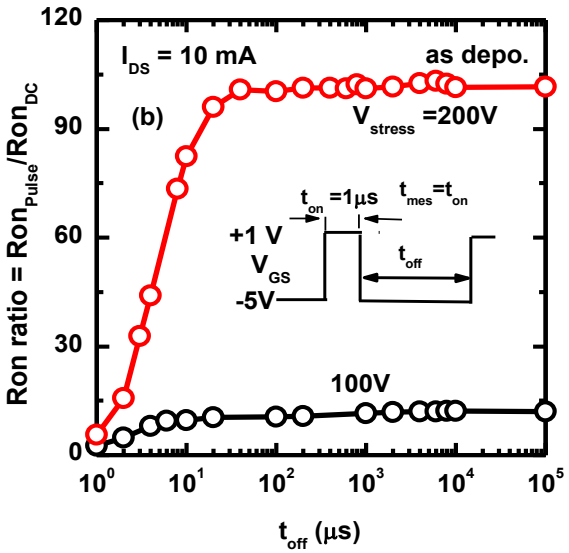


Fig. 4 Time dependent R_{ON} ratio for device A. On-state time (a) and off-state time (b).