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An Optical 0.25-µm GaN HEMT Technology on 100-mm SiC for RF Discrete and Foundry MMIC Products

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***Abstract* — A 0.25-µm, production III-Nitride-based high-electron mobility transistor (HEMT) technology on 100-mm SiC substrates is described. The base technology, G40V4, employs dielectric sidewall spacers to achieve 0.25-µm gate length and reliable 40-V operation. It demonstrates 7 W/mm CW output power at 10 and 14 GHz, while exhibiting f_T >25 GHz at 40 V and 10% I_{DSS} quiescent bias. Examples of discrete transistor and MMIC power amplifier designs using this 0.25-µm HEMT are presented.**

***Index Terms* — Gallium nitride, HEMT, HTRB, Ku-Band, MMIC, RADAR, SATCOM, Silicon Carbide, X-Band.**

I. Introduction

III-Nitride based High-electron-mobility transistors have several advantages over currently available technologies and will be dominant for use in future infrastructure installations. The GaN/AlN/AlGaN HEMT has a unique combination of high-current, high-f_T, and high breakdown voltage that enables high power performance over a wide frequency range [1]-[3]. For reliability concerns, all practical GaN HEMT device structures have adopted advanced peak electric field shaping on the drain side of the gate electrode. This is accomplished by using single or multiple field plate structures that are specifically engineered to maximize performance and reliability at a target frequency band of interest [4], [5].

Most released GaN-on-SiC technologies service commercial and military 28-volt applications very well in the dc to 6 GHz frequency range, depending on the technology's gate length. Examples include S-band radar and even have been demonstrated in advanced designs with harmonic terminations up through 2.3 GHz [6]-[8]. Despite the increasing use of this technology, gate lengths longer than 0.3 µm cannot service performance requirements for next-generation sensors and jammers. Higher f_T, more gain and higher voltage operation are needed to:

1) support new wide-band EW applications and higher frequency commercial markets (e.g., commercial V-sat, commercial backhaul transport);
2) take the typical S-band performance to an improved level for ultra-high efficiency capability of GaN in S-band radar applications [9];
3) support the higher peak power required in shorter pulse width, higher peak power apps like AEW airborne radar, L-band volume search radar, S-band TWT replacement programs.

As a result, a GaN/AlN/AlGaN HEMT has been developed with 0.25-µm gate length on SiC substrates to provide a higher-frequency, higher-voltage-capable device technology (G40V4). This paper describes the 0.25-µm device structure, process technology and performance and qualification data, as well as examples of released discrete and MMIC products designed and fabricated with this technology.

II. G40V4 GaN HEMT Technology Description

The epilayers for the GaN HEMTs described in this paper are grown by metal-organic chemical vapor deposition (MOCVD) in a multi-wafer, high-volume reactor on 100-mm semi-insulating 4H silicon carbide (SI 4H-SiC) substrates that are typically cut on-axis. The typical structure comprises an AlN nucleation layer, 1.4 µm of insulating GaN, approximately 0.6 nm AlN barrier layer, and a 25 nm cap layer of undoped $Al_{0.22}Ga_{0.78}N$. This nominal layer thickness and mole fraction yield sheet electron concentrations in the range of 8-10x10^{12}/cm^2, but due to the AlN interlayer, has the strong advantage of electron mobilities near 2000 cm^2/V-s at room temperature. The channel sheet resistance is about 335 Ω/□.

As shown in a schematic cross-section in Fig. 1, as is typical for released GaN processes, the base device is fabricated with SiN first passivation that is deposited by PECVD. Ohmic contacts are formed directly on the top AlGaN layer through openings in the SiN. Device isolation is achieved using a nitrogen implant to maintain a planar structure. A Ni/Pt/Au gate electrode is formed by straddling a

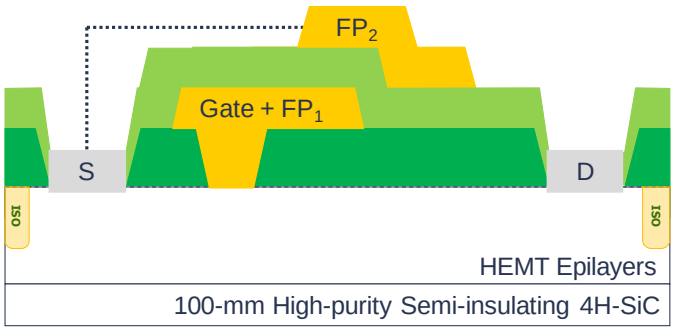

Fig. 1. Schematic cross-section of the AlGaN/AlN/GaN HEMT RF structure showing integrated 1st field plate and source-connected 2nd field plate. Dielectric passivation layers are PECVD-deposited SiN.

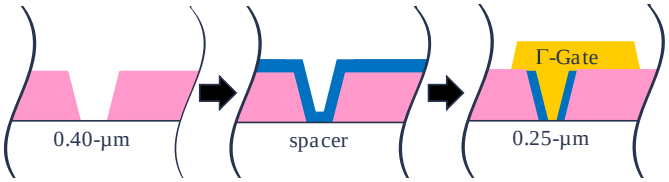

Fig. 2. Simplified process flow for Γ-gate formation for GaN V4, showing the method to achieve short optical gates.

dielectrically-defined (DD) opening in the first passivation to the AlGaN surface.

The G40V4 process employs a dielectric spacer method, which achieves short gates without serial printing of the gate pattern by costly and slow e-beam lithography [10]. The 0.25-µm spacer process flow is illustrated in Fig. 2. A repeatable 0.40-µm first opening is formed in the 1st passivation using i-line optical lithography and a flourine-based plasma etch. Subsequently, the first opening is narrowed using an isotropic deposition of a second dielectric, typically SiN, forming a sidewall spacer. The bottom part of the narrowed gate opening is removed with a controlled anisotropic etch to expose a much shorter length of AlGaN. With the first and second dielectric film thicknesses and first and second etch endpoint times under SPC control, the process produces a repeatable gate length. A control chart of the measured gate length is shown in Fig. 3, representing 18 months worth of data on a fully released foundry process.

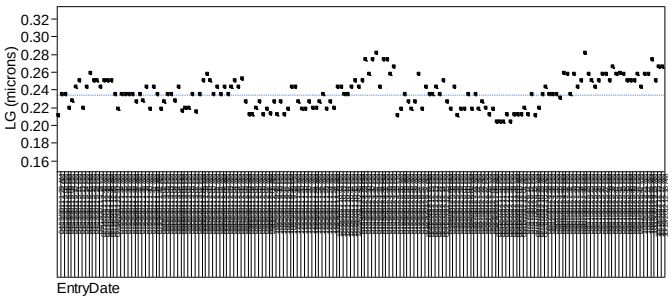

Fig. 3. 18 months of measured gate length data sampled on several wafers per wafer lot for the Cree V4 process.

Under RF operation, very strong peak electric fields occur at the drain-sided edge of the metal semiconductor junction in this lateral device. Thus, the optimized GaN device includes a lateral extension of the gate electrode on the drain side to provide an elegant integration of field shaping with the gate metallization (c.f. Fig. 1). It is typically called a "gamma gate" electrode and is an integrated "first field plate" [5]. The gate footprint is offset to reduce source resistance and increase gate-drain breakdown voltage. The gate-source spacing is nominally 1.0 µm, and the gate-to-drain spacing is about 3 µm. After a 2nd passivation, a source-connected 2nd field plate is fabricated to provide further electric field shaping at the highest drain voltages and to reduce gate-drain feedback capacitance of the device [5]. The source-connected 2nd field plate together with integrated 1st field plate has become the most widely used device structure in the industry for RF applications below 18 GHz. Using this optimized design, the 1-mA/mm breakdown voltage of this structure exceeds 120 V.

The unit-cell devices exhibit CW output power levels of 7 W/mm and PAE > 60% when measured under optimum load conditions at 40 V for both 10 and 14 GHz. Devices provide 15 and 12 dB of small-signal gain at 10 and 14 GHz, respectively. At the FET level, the G40V4 device provides f_T of >25 GHz at 40 V and at 10% I_{DSS} quiescent bias.

III. G40V4 Qualification Description

The G40V4 process technology fabricated on 100-mm wafers was qualified for volume manufacturing using a comprehensive set of acceptance tests on packaged discrete HEMT devices with 3.6 mm gate periphery. The devices were assembled using the production process using a 1:1:1 CuMoCu cavity-style package with AuSn eutectic die attach. High temperature operating life (HTOL) performed at 40 V, 225 °C, and 4 W/mm for 1000 h showed zero failures out of 75 devices sampled. In addition, the G40V4 process passes the 1000-h high-temperature-reverse-bias (HTRB) at 100 V, 150 °C, and V_G= -8 V with zero failures out of 75 devices sampled, demonstrating the excellent reliability of this technology, which has not been reported for other 0.25-µm GaN HEMT released processes. Finally, temperature cycling (TC) from 150 °C to -65 °C showed zero failures out of 75 devices sampled. No substantial device parametric shifts were observed after these qualification reliability tests. These results demonstrate excellent stability and reliability performance at operating conditions for the baseline G40V4 process technology.

IV. 0.25-Micron Discrete and MMIC Examples

Many applications exist for a high frequency, high voltage process above 6 GHz, including X-Band radar, C, X and Ku-Band Satellite communications, as well as PTP backhaul and other more niche industrial scientific and medical bands. With any application there is always a trade off of cost vs. performance, so discrete transistors and MMICs are being developed for these example applications.

A family of die engines has been developed to enable the design of chip-and-wire hybrids for applications up to 18 GHz. These die are all capable of operation at drain voltages

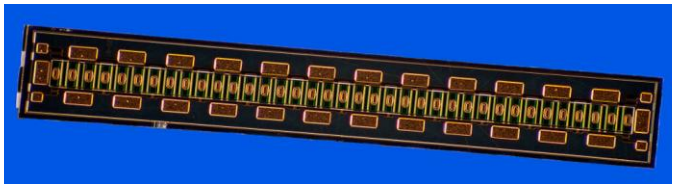

Fig. 4. A 70-W Ku-Band capable GaN HEMT die.

of 40 V and as such were optimized for good performance in challenging thermal environments. The initial family of die has output power capabilities of 6 W, 25 W and 70 W when rated at 85 °C. The thermal resistance of the 70 W die is about 1 °C/W when dissipating 6 W/mm. The entire die family is capable of providing 60% power added efficiency and greater than 17 dB small signal gain at 10 GHz.

The largest of these new 0.25-µm, 40-V die, pictured in Figure 4, has been designed into a fully matched transistor product operating at X-Band. The products CGHV96050F and CGHV96100F both cover the X-Band satellite communications band, 7.9-8.4 GHz, and also commercial marine radar applications up to 9.6 GHz. The 50-W product employs one 70-W die in an internally matched package format. The typical performance of this amplifier is shown in Figure 5. The performance achieved across the band is better than 11 dB associated gain with 50 % power added efficiency.

The 100-W product uses two of the 70-W die and was designed using the same matching networks as for the single ended product, with this design also including associated divider and combiner networks. The design challenges associated with a product of this complexity were such that all available simulation and analysis tools were used including; basic harmonic balance using a mature large signal model, planar electromagnetic simulations of the hybrid substrates and full 3-D electromagnetic simulations of the complex wire bonding networks and their interactions with the surrounding circuits. With the appropriate use of these tools, the performance shown for both of these products is representative of first pass design success. Typical performance of the 100-W transistor is shown in Figure 6. With greater than 140 W output power and an associated gain of > 10 dB and PAE of better than 40%, it is clear to see that our 0.25-µm, 40-V technology can enable very high performance amplifiers at X-band.

MMIC based amplifiers have also been developed using the

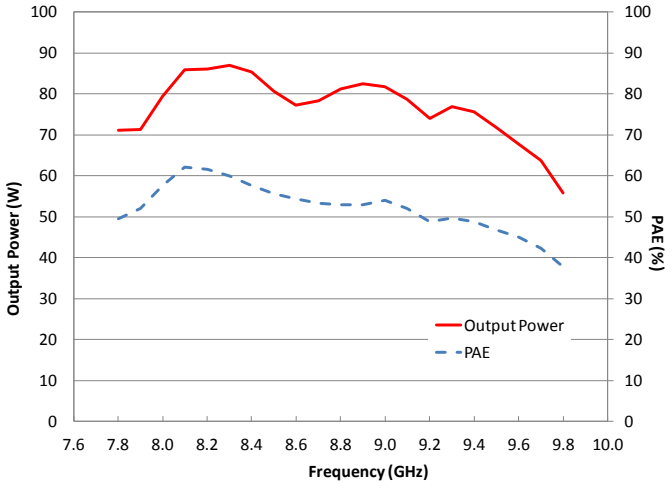

Fig. 5. Discrete Matched Transistor CGHV96050F – Measured output power and PAE.

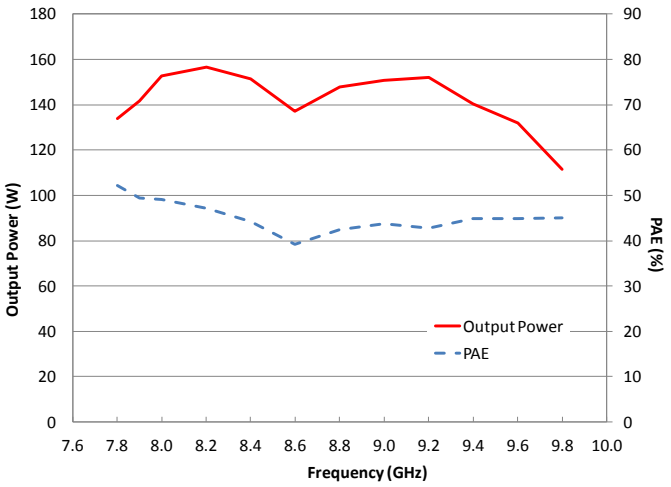

Fig. 6. Discrete Matched Transistor CGHV96100F – Measured output power and PAE.

V4 technology and previously proven GaN-on-SiC MMIC processing [9]. Bandwidth, performance and size are often drivers that require the use of MMIC based technology. An example of such a design that requires the ultimate in performance and size is a 6-12 GHz, 25 W, power amplifier. The power amplifier is a packaged transistor that uses a 3-stage reactively matched MMIC housed inside a metal ceramic package with associated integrated bypassing and dedicated bias leads. In this application, the MMIC was designed at 28 V for **CW** operation. The lower supply voltage was selected due to the severe bandwidth challenges which in turn leads to lower efficiency and thus thermal challenges. The measured performance of this MMIC is shown in Fig. 7. In summary, this product provides >25 W saturated output power at a case temperature of 85 °C with associated gain of 23 dB and power added efficiency of >20% over the entire band. The resulting packaged product is less than 0.058 cubic inches in volume and has external dimensions of 0.385”x1.0”x0.15”.

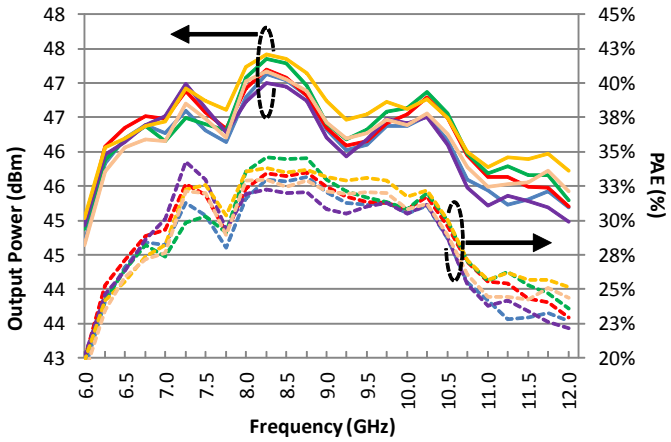

Fig. 7. Measured 6-12 GHz large-signal CW performance of several fixtured MMICs.

V. Conclusion

A manufacturable GaN/AlN/AlGaN HEMT MMIC with 0.25-µm gate length on 100-mm SiC substrates provides a higher-frequency, higher-voltage-capable device technology. It employs dielectric sidewall spacers to achieve 0.25-µm gate length and reliable 40-V operation, which can support new wide-band EW applications as well as improve performance of wide-band circuits at S-band. It demonstrates 7 W/mm CW output power at 10 and 14 GHz, while exhibiting f_T >25 GHz at 40 V and 10% I_{DSS} quiescent bias. Examples of discrete transistor and MMIC power amplifier designs using this 0.25-µm HEMT were presented.

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