Correct determination of trap densities at high-*k*/III-V interfaces

R. Engel-Herbert

Department of Materials Science and Engineering,
Pennsylvania State University, University Park, PA 16802, USA.

Over the past decades the continuous scaling of silicon based metal-oxide semiconductor field effect transistors (MOSFETs) has pushed the channel material to its intrinsic limits. To date, strain-engineering is utilized to reduce the effective mass of carriers in the channel. High-k/metal gate technology has been successfully implemented into the manufacturing process to maintain electrostatic control in highly scaled device. Currently advanced non-planar device architectures, such as FinFET structures, are being actively pursuit to enable high performance computing at lower operation voltages addressing the power constraints in existing CMOS technology.

In this regard, alternative high mobility, small band gap materials, such as III-V compound semiconductors, are becoming attractive to replace silicon as the channel material. InGaAs and Ge have been proposed as potential candidates for n and p-MOS devices offering higher carrier velocities and mobilities than Si [1] and antimonide based compound semiconductors are being pursued for p-channel transistors as well [2].

However, building MOSFETs using III-V semiconductors is accompanied by a set of challenges. One main roadblock is to find a suitable gate dielectric that is thermodynamically stable in contact with III-Vs, exhibiting a small interface trap density, and has a high dielectric constant. Developing a suitable gate stack technology for III-Vs while meeting the more stringent processing requirements, such as reduced thermal budgets and avoiding native oxide formation during high-k deposition limiting the exposure of the semiconductor surface to oxidizing atmospheres is therefore key to enable III-Vs as new channel materials in MOSFET technology.

A mandatory requirement to develop an understanding of interface trap formation during high-k/metal stack formation and the effectiveness of existing and newly developed surface passivation schemes to improve the high-k/III-V interface quality is to unambiguously and quantitatively extract trap densities located at the interface. However, for similar high-k/III-V MOS capacitor admittance responses reported in the literature interface trap densities (D_{it}) that differ by orders of magnitude were extracted. Even the application of different, well-established D_{it} extraction techniques to the same device gives markedly different results suggesting that the interpretation is not straight forward.

In this talk I will address the issues associated with the application of quantitative methods to determine interface trap densities at high-*k*/III-V interfaces using admittance measurements of MOS capacitor devices [3]. A comparison of the different quantitative methods will be presented and their individual advantages, shortcomings and possible pitfalls are discussed exemplarily for the HfO_2/n-$In_{0.53}Ga_{0.47}As$ interface. Guidelines will be derived that help avoiding misinterpretation of measured admittance responses. Recent

advances in the deposition of high-*k* dielectrics on III-Vs will be presented demonstrating that oxide capacitance scaling is achieved while keeping the interface trap density at acceptable levels.

[1] M. Heyns and W. Tsai, *"Ultimate Scaling of CMOS Devives with Ge and III-V Materials"*, MRS Bulletin **34**, 485 (2009).

[2] B. R. Bennett, M. G. Ancona and J. B. Boos *"Compound semiconductors for Low-Power p-Channel Field Effect Transistors"*, MRS Bulletin **34**, 530 (2009).

[3] R. Engel-Herbert, Y. Hwang and S. Stemmer *"Comparison of methods to quantify interface trap densities at dielectric/III-V semiconductor interfaces"*, J. Appl. Phys. **108**, 124101 (2010).