# GaN-on-SiC MMIC Production for S-Band and EW-Band Applications

Ryan Fury, Scott T. Sheppard, Jeffrey B. Barner, Bill Pribble, Jeremy Fisher, Donald A. Gajewski,
Fabian Radulescu, Helmut Hagleitner, Dan Namishia, Zoltan Ring, Jennifer Gao, Sangmin Lee,
Brian Fetzer, Rick McFarland, Jim Milligan and John Palmour
Cree Inc., 4600 Silicon Dr., Durham, NC 27703
Ryan_Fury@cree.com, Ph: (919) 407-7061, Fax: (919) 313-5696

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**Abstract**

**An overview of Cree's Title III production-capacity program for GaN-on-SiC MMIC on 100-mm-diameter substrates is presented. This program is focused on Manufacturing Readiness Assessments (MRA) of key metrics including reliability ($T_{50}$ and $T_1$) yield, cost, and cycle time. The final program requirement is a Manufacturing Readiness Level (MRL) of eight (8) or higher.**

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## I. Introduction

A program to develop high volume production capability for GaN-on-SiC MMICs is being executed at Cree, Inc. under funding from the Defense Production Act (DPA) Title-III Program. This program is a culmination of a previous Title-III program for conversion of SiC MESFET MMIC technology to 100-mm 4H-SiC substrates [1, 2] and a DARPA Wide Bandgap Semiconductor program that was dedicated to making GaN HEMT technology ready for reliable X-band power amplifiers [3]. Our 3-year program is organized into three main phases, including a baseline assessment, process improvement and final assessment where success is coupled with achieving Key Performance Parameters (KPPs) of technology reliability, yield, cost, and cycle time. The program has two main MMIC demonstrators: a 75 W S-Band and a 25 W EW-Band die. The die are fabricated with our G28V3 (0.4-µm gate length, 28-V) and G28V4 (0.25-µm gate length, 28-V) GaN HEMT processes for the S-Band and EW-Band die, respectively. A main goal of the program is to provide an open MMIC foundry for industry to benefit from the advantages GaN technology.

This paper gives an overview of the structure of the program, general descriptions of both the 0.4-µm gate length G28V3 process and 0.25-µm gate length G28V4 process, the current status of the MMIC test vehicles with respect to the Key Performance Parameters (KPPs), and finally the projected performance of the program compared to the MRL requirements.

## II. Technology Overview

Detailed descriptions of the G28V3 and G28V4 technologies are published elsewhere [3, 4]. Cree GaN HEMT MMIC technology is built upon III-Nitride epilayers grown by MOCVD on 100-mm high-purity-semi-insulating (HPSI) 4H-SiC substrates. Substrate manufacturing and GaN HEMT epitaxial growth are well-established commercially and have not been focus areas on the program. The primary thrust has been to realize the targeted MMIC KPPs. Both S-band and EW-band processes utilize the same production epilayer structure that comprises an insulating GaN buffer with AlN and AlGaN cap layers that yield a channel sheet resistance centered at 335 Ω/□. GaN MMICs utilize microstrip lines with standard passive components such as dielectrically-supported bridge metal, MIM capacitors, thin film resistors and through-wafer slot vias. The MIM capacitors support peak voltages over 100 V, and the source slot vias are implemented in the 4-mil SiC substrates to simplify the layout and increase gain [5].

As shown in a representative cross-section in Fig. 1, the defining features of the V3 and V4 technologies include a Ni/Pt/Au gate electrode that is formed by straddling a dielectrically-defined (DD) opening in the first SiN passivation to the AlGaN surface. The 0.4-µm V3 gate length is achieved with standard optical lithography and a single SiN etch, while the 0.25-µm V4 gate length is achieved using optical lithography and a standard sidewall spacer, which is illustrated conceptually in Fig. 2. Source-connected field plates are used for improving gain and RF power density, reducing peak fields in the device and thereby improving reliability and lowering feedback capacitance [6]. Dimensions of the passivation dielectrics and fieldplate structures are optimized for performance in

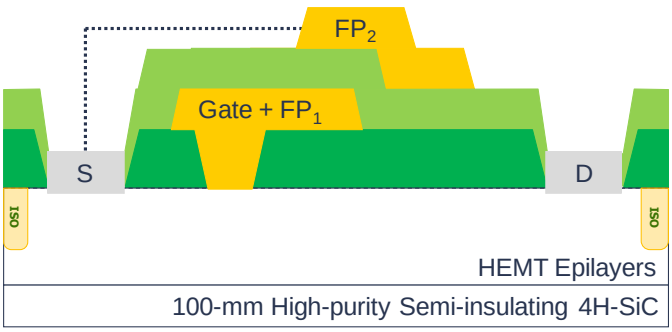


Fig. 1. Schematic cross-section of the AlGaN/AlN/GaN HEMT RF structure showing integrated 1st field plate and source-connected 2nd field plate. Dielectric passivation layers are silicon nitride.

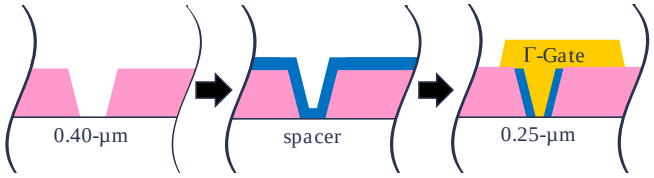


Fig. 2. Simplified process flow for Γ-gate formation for V4 GaN, showing the method to achieve short optical gates.

the respective frequency bands of use. The source-connected 2nd field plate together with integrated 1st field plate has become the most widely used device structure in the industry for RF applications below 18 GHz. Using this optimized design, the 1-mA/mm breakdown voltage of this structure exceeds 120 V for both V3 and V4 processes.

## III. Structure of the Program

The 3-year program is being executed in three main phases: Baseline Assessment, Refinement Improvement and Final Assessment. The Baseline and Final Assessment phases take place over the first and last year of the program respectively. The Refinement phase spans over the first two years of the program and concludes before the last phase to allow accepted production improvements to be rolled into the Final Assessment. The program has completed the Baseline Assessment and a number of significant process improvement projects. The Baseline Assessment phase validated the fundamental production cost, cycle time, yields and performance of the S-Band and EW-Band MMICs. The data collected from the baseline portion of the plan was used to confirm and update the program KPP. The Process Refinement phase is currently being executed to insure success in the Final Assessment phase. Process Control Review Board (PCRB) Refinement lots incorporate modifications to the process that improve manufacturability, yield, reliability, cycle time, and cost. The Final Assessment phase will consist of pilot production runs with updated MMIC PA mask sets that incorporate all the improvements in Cree's GaN V3 and V4 process that have been validated by the PCRB. Complete data will be obtained and used to validate the KPPs. Devices from these lots will be used to perform full three-temperature Arrhenius and qualification data.

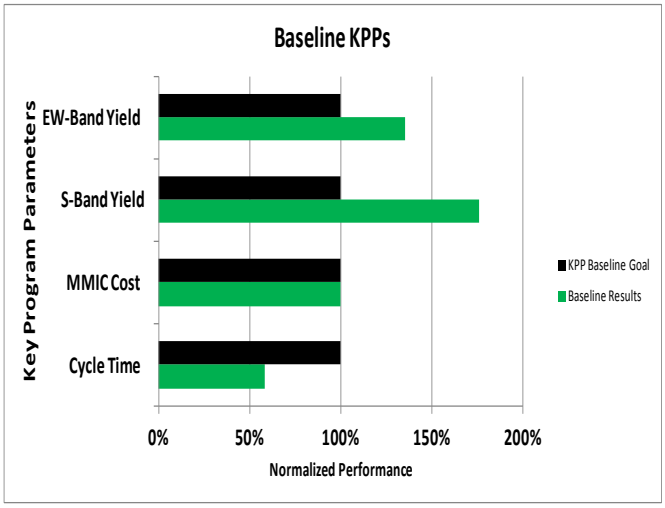


Fig. 3. Title-III GaN-on-SiC Program essential Baseline Key Program Parameters goals and corresponding results. As shown, an increase yields and reduction in cycle time exceed the goals.

## IV. Baseline and Refinement Results

The Baseline Assessment phase of the program used S-Band MMICs and EW-Band MMICs as vehicles to validate the Cree G28V3 and G28V4 processes, respectively, against the first-year KPP goals. The S-Band G28V3 MMICs are two-stage amplifiers designed for an operating voltage of 28 volts, a chip area of 22.57 $mm^2$, and a percent bandwidth of 26%. Also assessed in the Baseline phase are S-Band PCM reticles containing critical non-MMIC elements required to ensure compliance with the V3 process. The PCM reticles include S-Band SECs, dielectric crossover transmission lines, 3.6-mm FET SECs, RF MIMcaps, and inter-metal contact chains. The EW-Band G28V4 MMICs are three-stage amplifiers also designed for an operating voltage of 28 V, chip area of 28.43 $mm^2$, and a percent bandwidth of 100%. The EW-Band mask set also has PCM reticles with the same structures listed on the S-band PCM cells. Amongst the many KPP goals for each stage of the program, most important are the parameters that drive the yield, cost,

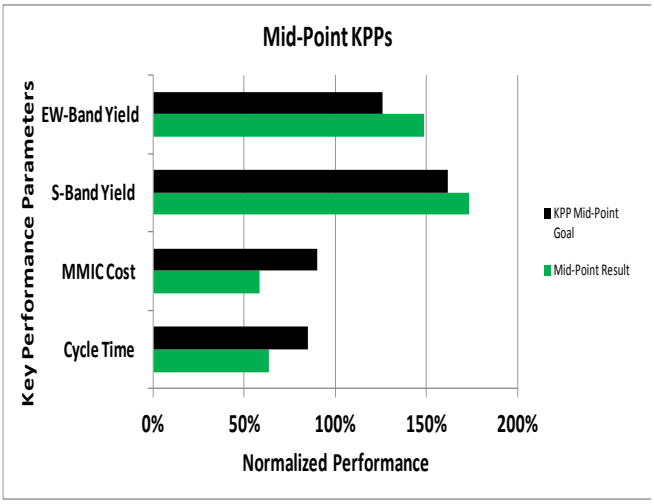


Fig. 4. Title-III GaN-on-SiC Program essential Mid-Point Key Program Parameters goals and corresponding results (normalized to the Baseline KPPs). As shown, an increase yields, reduction in cost, and reduction in cycle time exceed the goals.

and reliability of the technology. Net MMIC yield is a composite of line, on-wafer dc, on-wafer RF and post-singulation visual yields. Fig 3 shows the salient Baseline KPPs with the goals and normalized results. Between the S-Band and EW-Band MMIC yields, the results exceeded the goals up to 75% while the cycle time reduction surpassed the goal by 42%.

Cree's objective for the Refinement Phase was to further improve performance in each of the KPP areas. In order to establish a valid comparison against the Baseline Assessment lots, the Refinement phase used the same S-Band and EW-Band test vehicles while iteratively improving the process through refinement lots. Each iteration of the refinement lots modified different areas of the V3 and V4 process with the intention of gaining enhanced yields, performance, reduced cycle times, lower cost, and overall more favorable manufacturability. Early activity of the refinement phase focused on channel visual yield improvement by optimizing a gate metal electrode liftoff step specifically to reduce the number of damage sites. We also converted to a new post-backside de-bond process that reduced frontside damage significantly and reduced cycle time. Another refinement activity included qualification of the SiN passivation tool from a manually-loaded, older PECVD platform to an-automated, newer PECVD platform with reduced particle count, a more controlled process and process redundancy. The upcoming final refinement lot will aim at additional yield improvements to facilitate further cost reduction. Fig. 4 shows the improvements made thus far in the Refinement phase KPPs normalized results, which currently reflect the Mid-Point of the program. Again, the results indicate yield improvements better than the Mid-Point goal ranging from 8% on the S-Band to 18% on the EW-Band. In addition, the MMIC cost and cycle time resulted in a 36% and 25% reduction compared to the normalized KPP Mid-Point goal.

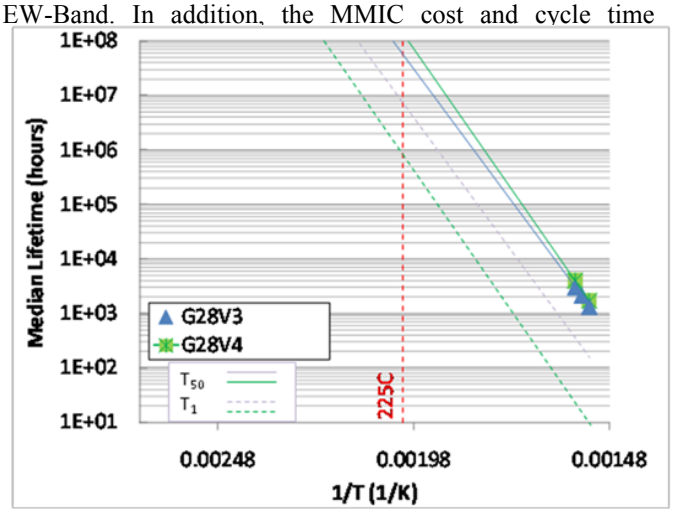


Fig. 5. G28V3 and G28V4 Process Arrhenius results with projections of the mean-time-to-failure (T50, upper solid lines) down to the 1%-tile failure projection (T1, lower dashed lines). The program requirements are fully met on these processes with a T50>1E6 h and T1>1E5 h.

Cree has performed a thorough MRA that takes into account all aspects of manufacturing, design, technology, quality and reliability by using the Air Force Research Laboratory MRL tool [7]. Specific to this program was inclusion of the yield KPP and the 1% time to fail projections. Figure 5 shows the intrinsic reliability data and lifetime projections for T50% and T1%, for the G28V3 and G28V4 processes. The results show that the intrinsic reliability performance exceeds the program requirements of T50% > 1E6 hours and T1% > 1E5 hours of continuous operation at 125 °C at the back of the MMIC die, which equates to a maximum junction temperature of 225 °C, or less, for normal operating conditions of the target applications. Both V3 and V4 technologies also successfully passed the 1000-h standard qualification tests of high-temperature operating life (HTOL) (28 V, Tj = 225 °C, and 4 W/mm) and high-temperature-reverse-bias (HTRB) (84 V, Tb = 150 °C, and VG= -8 V). This result demonstrates the voltage robustness of this technology, not typically reported for other released GaN HEMT processes. In Year 1 of the program, the G28V3 manufacturing process was assessed at MRL 8 with a production line capability of Low Rate Initial Production and the G28V4 process was assessed at MRL 7.

## V. Final Phase Goals

The primary goal of the program is to achieve MRL 8 on both the G28V3 and G28V4 processes during the Final

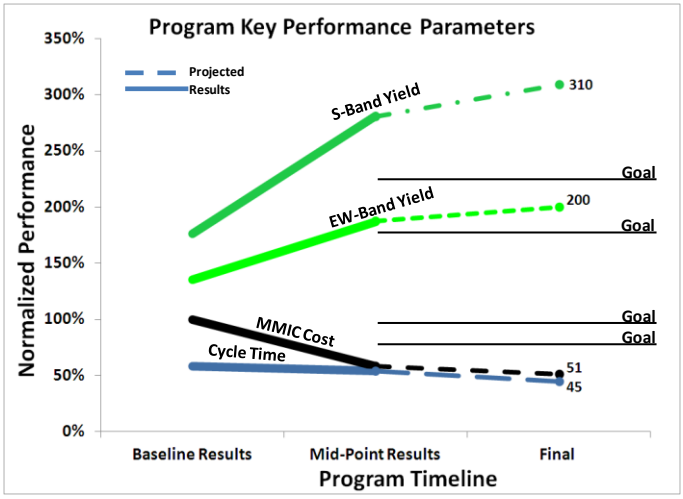


Fig. 6. Key Program Parameters of yield, cycle time and die cost normalized to program start. The solid lines are the program plan results while the dotted lines are the Final projections. Four horizontal lines indicate the Final phase goals. As can be seen, all KPPs are currently above the plan with a projection exceed far beyond goals.

Phase. Fig 6 illustrates both the current performance of program (thick lines) while the Final Phase section shows not only the projected performance (dashed lines) for the KPPs at the conclusion of the program but a comparison of performance normalized to the Final Phase KPP goals created at program kickoff. As illustrated, Cree fully intends to surpass each KPP goal by a wide margin.

Along with further improving the production parameters such as yield, MMIC cost, and cycle time, the program has the goal of validating the intrinsic reliability data for the V3 and V4 technologies and proving the robustness of V3 and V4 through a 8000-h RF HTOL. At the completion of the Final Phase Assessment lots, Cree will take a randomly selected subset of parts for a two temperature Arrhenius test and a 8000-h RF HTOL and provide further confidence in the V3 and V4 process beyond what is established during the Refinement Phase.

## VI. Conclusion

Cree has provided Baseline and Refinement Phase results outperforming initially set goals while summarizing the remaining steps to establish optimal KPP projected performance. Potential foundry customers can already gain significant advantages in MMIC costs, yields, and cycle times realized under this Title III program. The improvements planned for the remainder of the program will enable Cree to achieve the primary objective of verifying a production capability with a MRL of 8 or low rate initial production (LRIP).

## Acknowledgements

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## Acronyms

KPP: Key Performance Parameter
LRIP: Low Rate Initial Production
MIMcap: Metal Insulator Metal Capacitor
MMIC: Monolithic Microwave Integrated Circuit
MRA: Manufacturing Readiness Assessment
MRL: Manufacturing Readiness Level
PCM: Process Control Monitor
PCRB: Process Control Review Board
SEC: Standard Evaluation Circuit