Impact of crystal-quality improvement of epitaxial wafers on RF and power switching devices by utilizing VAS-method grown GaN substrates with low-density and uniformly distributed dislocations

Yohei Otoki[1], Takeshi Tanaka[1], Hiroyuki Kamogawa[1], Naoki Kaneda[2], Tomoyoshi Mishima[2], Unhi Honda[3],and Yutaka Tokuda[3]

[1] Hitachi Cable, Ltd., Isagozawa 880, Hitachi City, Ibaraki 319-1418, JAPAN

[2]Corporate Advanced Technology Group, Hitachi Cable, Ltd., Tsuchiura 300-0026, JAPAN

[3] Department of Electrical and Electronics Engineering, Aichi Institute of Technology Yakusa, Toyota 470-0392, JAPAN

e-mail:yohei.otoki.pd@hitachi-cable.com

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Abstract *Impact of using low dislocation density GaN substrate grown by VAS (Void Associated separation) method on GaN-HEMT epi-wafer was investigated with regards to the point defects in the crystal. We found several hole and electron traps in the GaN crystals and each of concentration were sensitive to growth condition of epitaxial layers. There was no significant difference in the basic electrical properties such as buffer leakage current, sheet carrier density and mobility of GaN-HEMT epitaxial layers grown on SiC substrates compared to those on grown on GaN substrate with low-density and uniformly distributed dislocations using VAS method. However, photo luminescence (PL) of GaN epi-layer grown on GaN substrates showed a very high near band edge emission (NBE) and low "yellow band (YL)", which is known to come from some unknown defects in the bulk and affects a non-linear behavior of the transistors. This indicates that lower density of point defects on GaN substrates can improve the device performance. Very high breakdown of over 3000V is obtained from the p-n junction diode also grown on VAS GaN substrate.*

INTRODUCTION

Development of high performance GaN-HEMT power devices have been struggling with non-liner effects like current collapse, drain lag and gate lag. These effects are thought to come from (1) defects or damages induced by the device fabrication process at the surface i.e. dry etching and metal and/or passivation layer deposition, and (2) various traps in the material; especially, in the epi layers. Since the surface preparation has improved significantly prior to epi growth, the most of the traps are likely from bulk material. The density of traps is strongly affected by growth condition as well as type of reactor system. The growth technique of the epitaxial wafer must be reproducible. The recent improvements in crystal growth technology have allowed us to use quality crystals in investigation.

The origin of the traps in the crystal, causing the non-leaner effects, can be divided into two groups; a) residual or doped impurities such as carbon, iron, and oxygen and b) point defects like vacancies, interstitials, anti-sites, and their complex. We reported about the behavior of Carbon and Iron by lights-induced current method in the last conference[1] and we can see some other reports about these impurities[2]-[4]. The role and character of the point defects, however, are totally not clear yet, because the GaN epi layers have too many defects as well. The most well-known defects are dislocations whose density is typically over 1E8-1E10 cm^{-2} for epi-layers on hetero-substrates like Si, sapphire and SiC. To clarify the effect of dislocation, we used GaN substrate grown by VAS method[5][6], where dislocation density is quite low (< 3E6cm^{-2}) and uniformly distributed in a wafer both microscopically and macroscopically. This uniformity enables us to have stable and accurate characterization. The quality difference of epi-layer on SiC substrate and on VAS-GaN substrates are discussed from view point of traps and potential performance of device.

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EXPERIMENTS & RESULTS

1. Characterization of deep levels in GaN grown in different growth condition

First, deep levels in the epi-layers grown by different growth conditions were measured by DLTS for electron traps and MCTS (minority carrier transient spectroscopy)[4] for hole traps to clarify what kinds of traps have in the GaN crystals and the effect on growth conditions. The samples were n-*type* GaN epi layer grown by MOCVD method[7][8] with different growth conditions (condition A and B) on semi-insulating SiC substrates. Carbon concentration of sample A was relatively high around 1E17cm^{-3} and that of B was as low as 2-5E16cm^{-3}. The results are shown in Fig.1, where four kinds of electron traps: E1, E2, E3, and E4 are observed in both samples A and B and each of those traps had large differences. Sample B had high E3 and low E2, but sample A had low E3 and high E2. The MCTS signals coming from hole traps also showed clear differences of the two samples. The hole trap concentration of sample A was much larger than that of sample B as shown in Fig.2. Summary of all the observations is shown in Table.1. These traps may cause some of non-liner effects on devices.

It's not clear if all the differences are only coming from carbon or not, because hole traps from low carbon sample was also reported [4]. However, one thing is clear that generation of traps is influenced by growth conditions. The growth conditions includes nominal temperature, temperature uniformity in a chamber, carrier gas (Hydrogen and/or Nitrogen), reactor pressure, growth rate, III/V ratio, gas flow system (perpendicular or horizontal), distance between gas outlet to substrate, formation of nucleation layer, and etc... Regarding to the relationship between trap and growth, a further study is necessary.

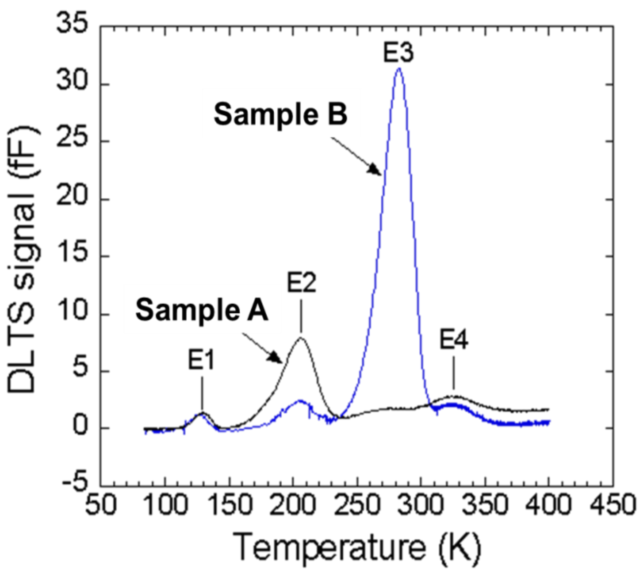


Fig.1 DLTS signals of sample A and B

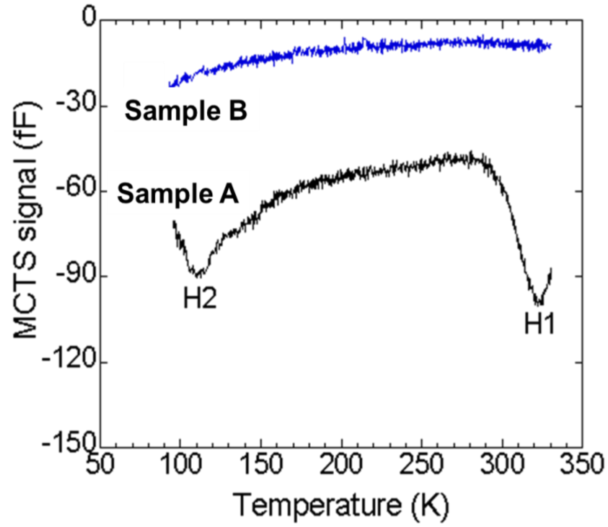


Fig.2 MCTS signals (showing hole traps) of sample A and B

Table 1. Energy levels, capture cross section, and trap concentrations in n-GaN by DLTS and MCTS.

Trap	Energy level (eV)	Capture cross section (cm^2)	Trap concentration (cm^{-3}) SanpleA	SampleB
E1	E_c-0.24	1.4×10^{-15}	5.5×10^{13}	6.6×10^{13}
E2	E_c-0.40	1.4×10^{-15}	1.2×10^{14}	3.4×10^{14}
E3	E_c-0.61	5.5×10^{-15}	2.1×10^{15}	9.5×10^{13}
E4	E_c-0.73	1.4×10^{-14}	1.7×10^{14}	1.9×10^{14}
H1	E_v+0.86	7.1×10^{-14}	1.8×10^{14}	2.2×10^{15}

2. Dislocation distribution of VAS GaN substrate

The dislocation density and its distribution of VAS GaN substrate were measured by CL (Cathode luminescence) method[3] as shown in Fig.3. The dislocation density was around 3E16cm^{-2}, which is two or three orders lower than that of epi-layer on SiC/sapphire/Si substrate. The dislocation was quite uniformly distributed macroscopically and microscopically in a wafer as shown in Fig.3 and Fig.4, respectively. Most of GaN substrates grown by other methods have inhomogeneous distribution of dislocation, with high and low density areas scattered in a wafer. This excellent uniformity of dislocations with low density in VAS-method GaN gives us stable and reliable results in experiments as well as high yield of devices in the mass production.

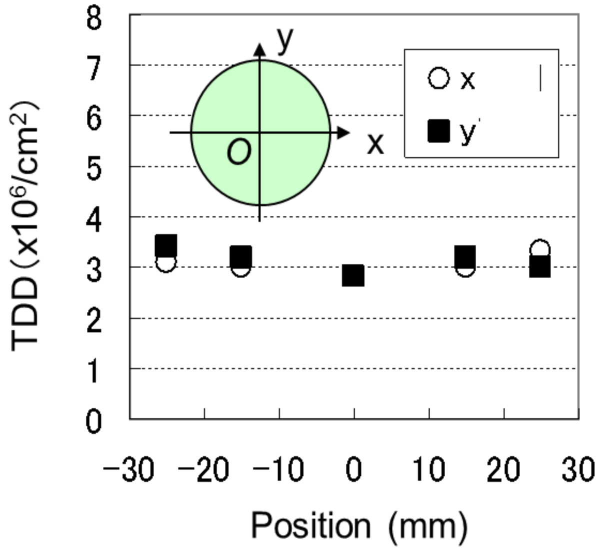


Fig.3 Dislocation density and its distribution of VAS method GaN substrate

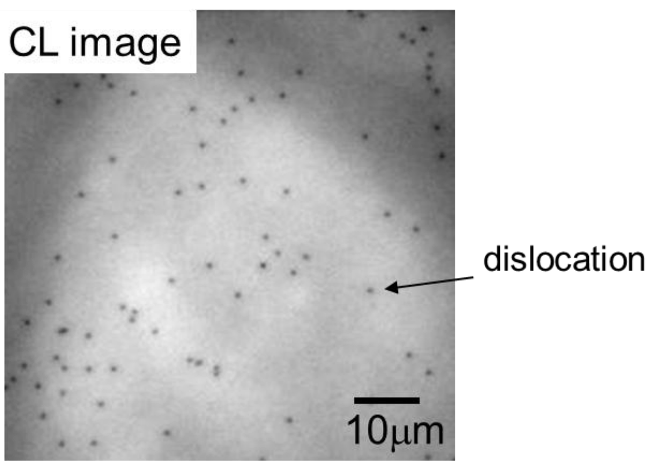
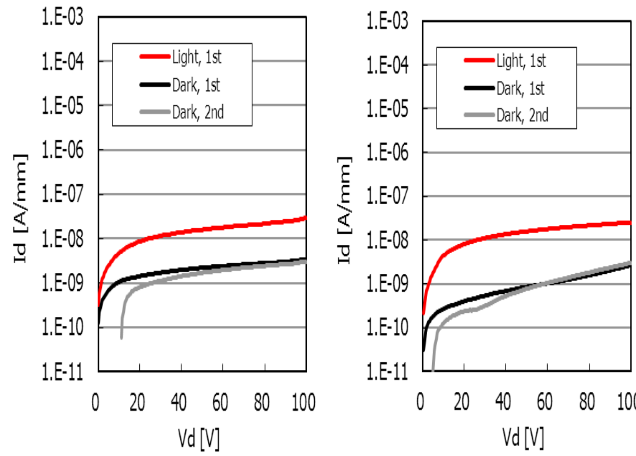


Fig.4 Microscopic distribution of dislocations of VAS method GaN substrate.

3. Properties of GaN-HEMT epi-wafer on SIC and VAS GaN substrate

The high resistive single layer was grown on SiC and GaN substrates under exactly same growth condition and the I-V curve under different color LED illumination [6] were measured. Significant difference was not found between layer on SiC and GaN as shown in Fig.5. The behavior seems to be dominated by major impurities like carbon, iron, and oxygen. Crystal point defects, like vacancy, antisite, interstitial and their complex, cannot be the "main" parameter to determine the leakage. It can be said the control of impurity concentration is essential to control the leakage level. The influence of point defects on leakage itself seems to be minor, if any, in this case.



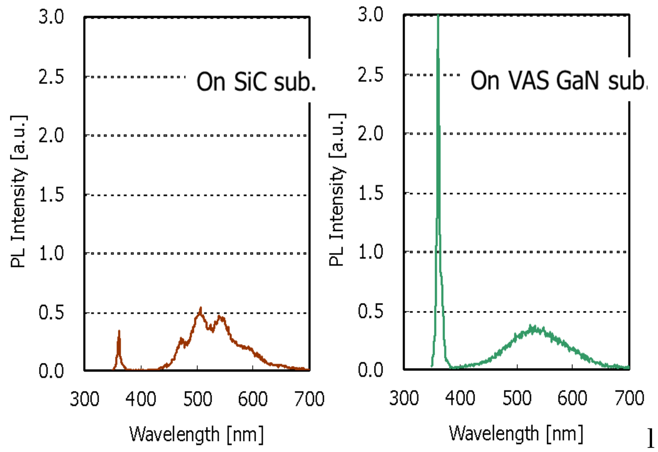
(a) iGaN layer on GaN (b) iGaN layer on SiC

Fig.5 Buffer leakage of GaN layer on GaN substrate and SiC substrate

The GaN-HEMT structures on these substrates were grown. No significant difference was also observed in the basic "major" properties like sheet carrier concentration and mobility. But PL profiles on GaN substrates showed very high band emission and lower, so called, "yellow luminescence" as shown in Fig.6, which is said to come from some unknown defects and affects the non-linear behavior of the transistors[9]. This remarkable result indicates the lower density of the defects in the GaN crystal grown on VAS-GaN substrate has high possibility of device performance improvement. Further experiment on this view points is going to be done.

Table 2 Properties of GaN HEMT epitaxial wafer grown on semi-insulating SiC substrate and semi-insulating VAS method GaN substrate

	Rs (ohm.cm)	Mobility (cm^2/Vs)	ns(2DEG) cm^{-2}
on SI SiC	608	1,790	5.7E+12
on SI GaN	521	1,690	7.1E+12



(a) (b)

Fig.6 PL profile of GaN-HEMT-epi grown on SiC and VAS GaN substrate by same growth condition

4. High breakdown p-n diode

Based on these results, the GaN p-n diodes (Fig.6) were fabricated[10] using the VAS-GaN substrate with uniform defect distribution which helped improve and stabilize the performance of these devices. The extremely high breakdown voltage, over 3000V, was obtained using very large electrode over 400um diameter[11]. This result promises the high possibility for the GaN bipolar transistor GaN with very high performance.

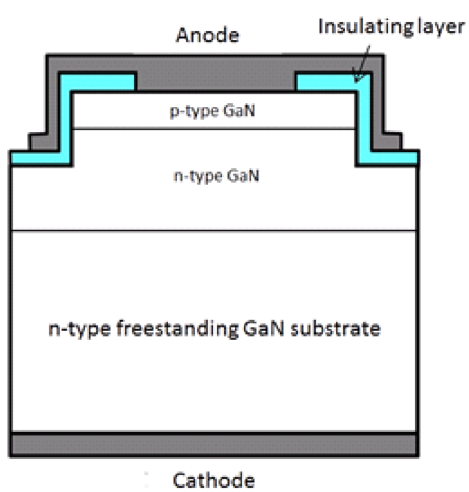


Fig.7 Cross section of P-N diode.

SUMMARY

Several hole and electron traps were found in the GaN crystals and each of traps concentration were sensitive to the influence of growth condition of epitaxial layers. The basic properties, such as buffer leakage current, sheet carrier density and mobility were shown almost same between GaN-HEMT epi-wafers on SiC and VAS-method GaN substrates. However, the PL result obtained from GaN substrates exhibited very high NBE and relatively low YL emissions. This indicates that the low density of dislocation in epi-layer on GaN substrates has a high possibility of device improvement such as a linearity. Very high breakdown voltage, over 3000V, was obtained from the p-n junction diode grown on VAS GaN substrate. These results suggested that the high performance of GaN bipolar devices can be achieved by using the VAS GaN substrate.

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ACRONYMS

GaN: Gallium Nitride
VAS: Void Associated Substrate
HEMT: High Mobility Electron Transistor
SiC: Silicon Carbide
DLTS: Deep Level Transient Spectroscopy
MCTS: Minority Carrier Transient Spectroscopy
MOCVD:Metal Organic Chemical Vapor Deposition
PL: Photo Luminescence
LED: Light Emitted Diode
CL: Cathode Luminescence