Effect of sputtered SiN passivation on current collapse of AlGaN/GaN HEMTs

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Abstract

The effects of sputtered SiN on current collapse of AlGaN/GaN HEMTs have been studied. The current collapse in terms of dynamic on-state resistance was reduced with increasing SiN deposition and post annealing temperatures due to the reduction of SiN/AlGaN interface trap density. These results indicate that sputtered SiN with deposition temperature at 250 °C is a promising candidate for passivation of AlGaN/GaN HEMTs.

INTRODUCTION

GaN-based HEMTs promise high power and high frequency operation due to the material advantages such as high breakdown field, high electron mobility, and high electron saturation velocity. A critical requirement in power electronics is to obtain a low resistance (R_{ON}). Even though many progresses have been achieved, there still remain some issues especially dynamic on-resistance degradation or current collapse which seriously limits the switching performance [1-3]. Although significant improvements have been achieved by various approaches such as surface passivation [4] and surface charge control with GaN cap layer [5], it is still a critical issue to understand and improvement of the current collapse. In this work, effects of sputtered SiN passivation with different deposition temperatures on current collapse have been studied by monitoring the dynamic change in R_{ON}. The ratio of R_{ON} is also measured in terms of post annealing temperature.

EXPERIMENTAL PROCEDURE

Figure 1 shows the schematic diagram of an AlGaN/GaN HEMT fabricated on a c-plane 3-inch sapphire substrate. Epitaxial layers were grown by metal-organic chemical vapor deposition (MOCVD) system. The structure consists of an undoped 1 μm thick GaN channel and an undoped 25 nm $Al_{0.25}Ga_{0.75}N$ barrier. Planar-type HEMT devices were fabricated by evaporating Ti/Al/Mo/Au as ohmic electrodes and Ni/Au as Schottky electrodes. The gate-to-source (L_{gs}) distance, gate length (L_g) and gate-to-drain (L_{gd}) distance were 2, 3, and 10 μm, respectively. The gate width was 200μm. Four types of devices were fabricated having passivation layers of SiN with different deposition temperatures, i.e. 100, 150, 200, and 250 °C (defined as device A, B, C, and D, respectively) for controlling the surface condition. SiN passivation layer was deposited by sputtering with a thickness of 150 nm. The maximum drain currents were almost the same (around I_{DSmax}=380 mA/mm) for the four devices at V_{GS} = 1 V. For device A, post annealing was performed at temperature from 300 to 500 °C for 10 min in N_2 ambient. The on-state resistance for DC, $R_{ON(DC)}$ was measured at constant drain current (I_{DS}) of 10 mA and V_{GS} = 1 V without stress voltage (V_{stress}). The dynamic on-state resistance, $R_{ON(pulse)}$ was measured at a constant I_{DS} of 10 mA and at V_{GS} = 1 V, using pulsed conditions with an on-state time (t_{on}) of 1μs and an off-state time (t_{off}) of 1ms. The bias pulse was applied from off-state (V_{GS} = -5 V with drain bias, V_{stress}) to on-state (V_{GS} = 1 V with constant I_{DS} = 10 mA). In order to keep I_{DS} constant, the load resistance (R_L) was varied. The current collapse or R_{ON} ratio was defined as R_{ON}(pulse)/R_{ON}(DC). All the devices were measured at room temperature and in the dark.

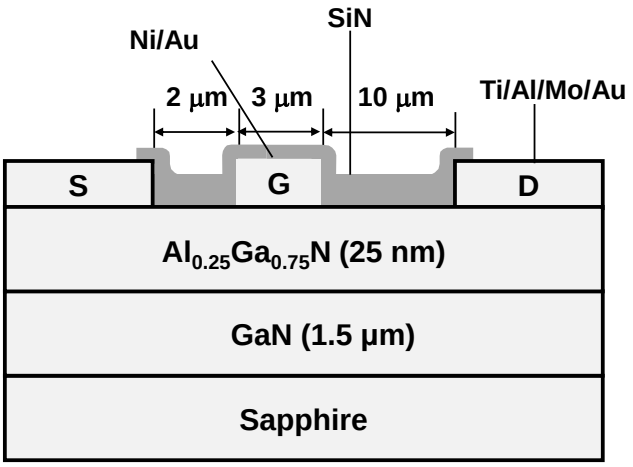

Fig.1 Schematic cross-sectional structure of $Al_{0.25}Ga_{0.75}N$/ GaN HEMT on sapphire substrate.

RESULTS AND DISCUSSION

Figure 2 shows the deposition temperature dependence of R_{ON}(DC). The R_{ON}(DC) was almost same for the deposition temperature. Figure 3 shows R_{ON} ratio as a function of deposition temperature. The R_{ON} ratio was decreased with

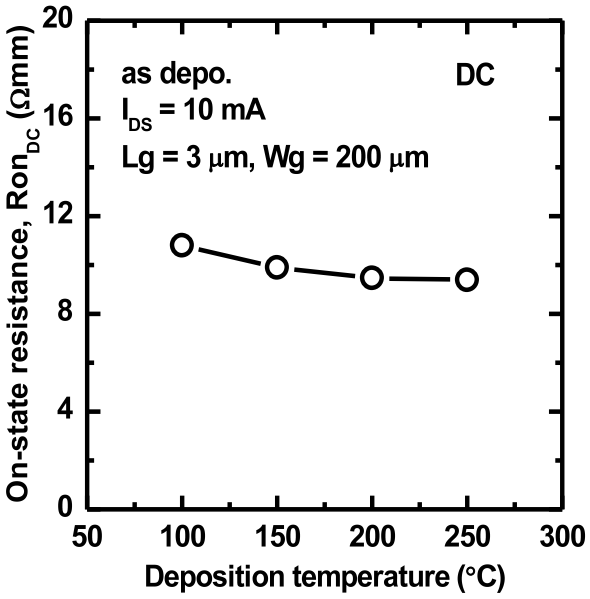

Fig. 2 On-state resistance, R_{ON}(DC) vs. deposition temperature.

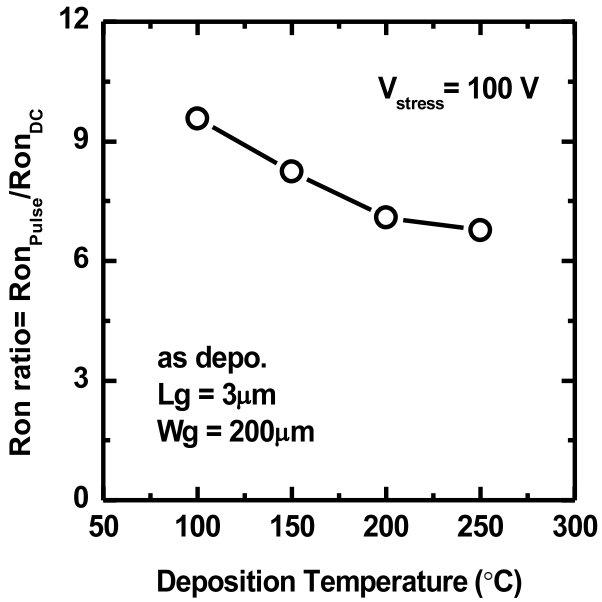

Fig. 3 R_{ON} ratio as a function of deposition temperature.

increasing the deposition temperature. Device A showed high R_{ON} ratio as compared to other devices. The dynamic R_{ON} increases in a prominent manner in all devices presumably as a result of the increased extension of the high field region into the drain. The R_{ON} is expressed as

$$R_{ON} = 2R_C + R_S + R_{CH} + R_D,$$

where R_C is the contact resistance (source contact and drain contact), R_S is the source resistance, R_{CH} is the channel resistance, and R_D is the drain resistance. The devices were fabricated on the same wafer and cut into four pieces for deposition of SiN passivation layer with different temperatures. Therefore, the R_C and R_S were the same for all the devices. The increase in R_{ON} ratio is brought from the change of R_{CH} and R_D. If traps exist between gate and drain, it may be possible to the change of R_{CH} and R_D. As a result, the increase of trap density increases the R_{ON} ratio. These results indicate that the trap density is reduced with the increase in deposition temperature.

Device A showed high R_{ON} ratio as compared to other devices. So, post annealing was performed for device A at temperatures from 300 to 500 °C for 10 min in N_2 ambient. Figure 4 shows the effect of post annealing temperature on R_{ON} ratio. The ratio of R_{ON} was decreased with the increase of annealing temperature. These results also indicate that the trap density is reduced with increasing the post annealing temperature.

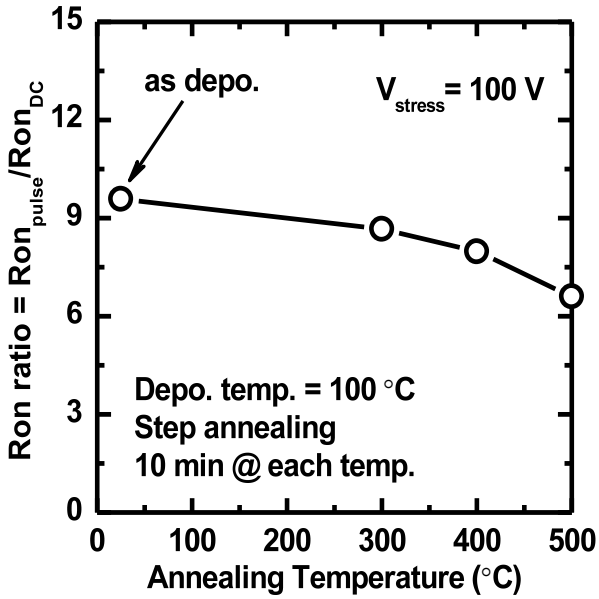

Fig. 4 R_{ON} ratio vs. annealing temperature.

Time dependent dynamic on-state resistance was also measured. The dependence of R_{ON} ratio vs. t_{on} and t_{off} were shown in Fig. 5. The R_{ON} ratio was decreased with increasing t_{on} for a fixed t_{off} of 1 ms (Fig. 5 (a)), while it was increased with increasing t_{off} for a fixed t_{on} of 1 μs (Fig. 5 (b)) for device A. Other devices were measured but not shown here. Figure 5 (a) and (b) are related to emission and capturing of trapped electrons, respectively. These results suggest that there are at least two distinct mechanisms that dominate dynamic R_{ON} ratio transients at short time and at long time. The long time transient is associated with the

same traps for all the devices, while the noticeable differences have been found at the short time. The short time transient may be associated with an intrinsic aspect of the deposition temperature of sputtered SiN and all devices suffer from it. The R_{ON} ratio recovery time was found to be decreased with the increasing in deposition temperature. Device A had slower R_{ON} ratio recovery time as compared to device D (not shown here). These results also imply that the electron trap density is reduced with increasing the deposition temperature.

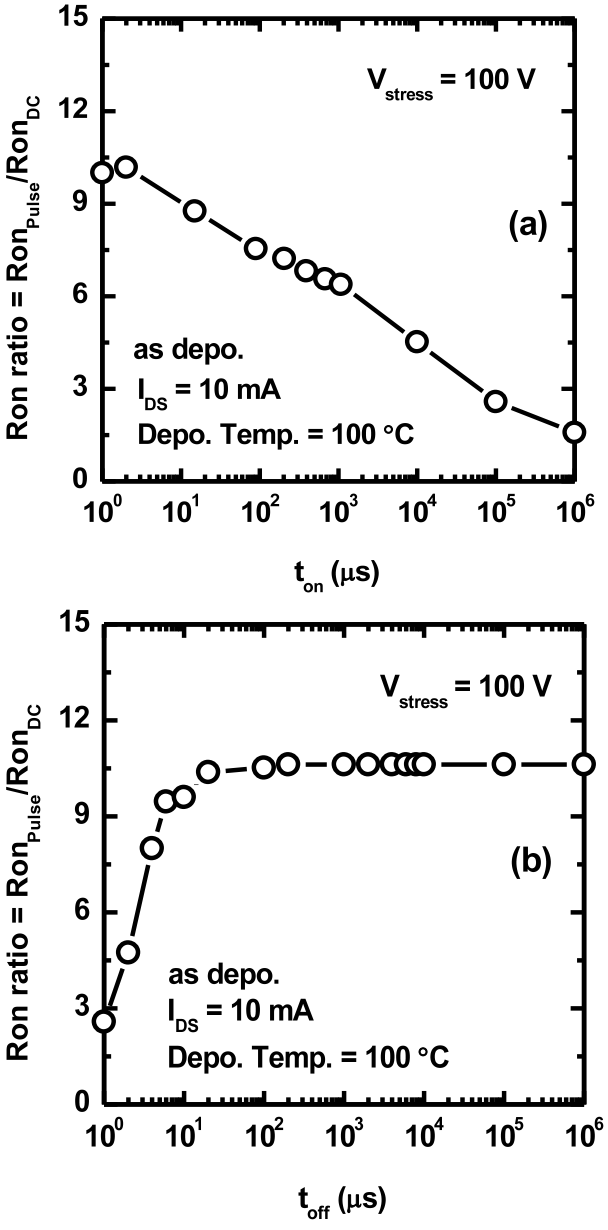

Fig. 5 R_{ON} ratio transients for device A. On-state time (a) and off-state time (b). At on-state time dependent measurement, t_{off} was fixed 1 ms and off-state time, t_{on} was fixed 1 μs.

The location of the trap is very important to analyze the trapping effect. The probable locations of electron traps are: (i) SiN/AlGaN interface, (ii) AlGaN layer, and (iii) buffer GaN. As all the devices have been fabricated on same wafer, it clearly suggests that the increase of dynamic R_{ON} is originated from surface traps and not related to buffer GaN traps. There is a possibility to contribute dynamic R_{ON} for traps in AlGaN layer, but SiN/AlGaN interface traps are dominated due to the change in surface conditions. At off-state, electrons were assumed to be injected from gate to SiN/AlGaN interface traps near the gate edge of a drain side under a large horizontal electric field. When device switched from off-state to on-state, it took time to emit trapped electrons. Therefore, dynamic R_{ON} was increased at short time. While the R_{ON} ratio was higher for device A as compared to device D, these results suggest that the electron trap density at SiN/AlGaN interface is higher for device A in comparison with that of device D. From above results, it can be concluded that current collapse was reduced by increased of the SiN deposition and post annealing temperatures.

6 a

CONCLUSIONS

The effect of SiN passivation on dynamic on-state resistance has investigated. The dynamic on-state resistance was measured after applying high drain voltage at off-state. Current collapse was decreased with increasing SiN deposition temperature. It was also decreased with the increase in annealing temperature. These results indicate that the SiN/AlGaN interface trap density is reduced with increasing the sputtered SiN deposition and post annealing temperatures.

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ACRONYMS

HEMT: High Electron Mobility Transistor
R_{ON}: Switch-ON resistance
R_{ON} ratio: $R_{ON(pulse)}/R_{ON(DC)}$ (Collapse factor)
V_{stress}: Stress voltage is applied between source to drain at off-state.