A New High Power GaN-on-Diamond HEMT with Low-Temperature Bonded Substrate Technology

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Abstract

We describe a low thermal resistance GaN-on-Diamond HEMT which can operate more reliably at a significantly lower junction temperature and is capable of providing >3X more power per unit chip area than the conventional GaN HEMT. Unlike the conventional high temperature bonded GaN-on-Diamond HEMT, a new low temperature diamond bonding process is developed to fabricate the device to minimize the impact from GaN/diamond coefficient of thermal expansion (CTE) mismatch. The low temperature bonding technology also allows the device to be fabricated prior to the diamond bonding, avoiding wafer bow issues. The new device is ideally suited to wideband electronic warfare (EW) PAs as they are the most thermally challenging – typically operated CW at very high power with lower efficiencies than narrowband amplifiers.

INTRODUCTION

Size, weight and power (SWaP) constraints significantly exacerbate the thermal management problem in military systems - as chips move to higher power levels, the need to design smaller electronic packages with these more powerful components fitting into tighter spaces makes thermal management very challenging. Since heat adversely affects both the performance and reliability of electronics, good thermal management through reductions in components' bulk and interface thermal resistances are of the utmost importance for military applications.

In most modern military electronic systems, the electronic device is typically the warmest element in the system. Although the thermal resistance of many military high-power electronic components can be as large as that of the remaining elements of the system combined, spreaders, heatsinks or coldplates do not directly access the active region where heat is generated, and cannot materially affect the device junction temperature. Since the junction temperature of a power transistor is dominated by the intra-chip heat spreading capability, to lower the device temperature one needs to place materials with high thermal conductivities immediately adjacent to the hot spot of the chip.

In this paper, we describe an innovative approach of placing the very high thermal conductivity diamond within 1μm of the hot spot (near junction) in a high power GaN HEMT. With this GaN-on-Diamond HEMT, one expects that the GaN device thermal resistance can be reduced, allowing the device to run cooler and therefore more reliably and efficiently. The power performance of the GaN technology is also projected to be significantly improved.

NEXT GENERATION HIGH POWER GAN TECHNOLOGY

The intrinsic properties of gallium nitride (GaN) make it an inherently superior material to silicon (Si) and gallium arsenide (GaAs) for high power electronic applications. However, full realization of the superior potential of GaN is limited by the thermal conductivity of the GaN epi layer and substrates on which GaN is grown. Commercial substrates for GaN epi layers include sapphire, Si and silicon carbide (SiC). These substrates have thermal conductivities between 40 and 400W/m-K. With thermal conductivity up to 2,000W/m-K, chemical vapor deposited (CVD) poly-crystal diamond can provide GaN with a substrate that has far superior heat spreading properties compared to that of SiC or any other commercially available substrate. Consequently, engineered wafers in which GaN epi layers are atomically attached to CVD diamond substrates, referred to as GaN-on-Diamond wafers (shown in Figure 1), offer potentially optimal heat spreading for GaN devices [1].

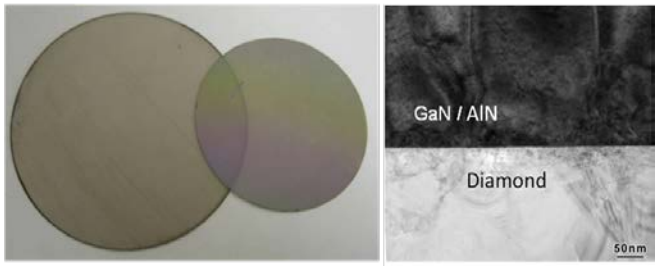

Figure 1. Left: 3" and 4" GaN-on-Diamond wafers. Right: high quality interface of high-temperature bonded diamond substrate/GaN HEMT epi. (From Group4 Labs, Ref 1)

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As shown in Figure 2, GaN epi bulk thermal conductivity, interfaces and substrate material play a significant role in device temperature rise. Consequently, due to its high thermal resistance, the GaN HEMT typically dominates the temperature rise in a power module. The way to improve heat flow from a device sub-micron hot spot is to spread it into the material surrounding the heat source. Placing materials with very high thermal conductivity diamond immediately adjacent to the hot spot can achieve exactly that. In this work, we proposed a new device structure, depicted in Figure 3, to achieve a quantum improvement in device thermal performance. Based on simulation, the new GaN-on-Diamond HEMT is projected to reduce channel temperature by ~40°C for the same operating conditions (P_{diss}). Figure 4 compares the new GaN-on-Diamond device to the conventional GaN-on-SiC HEMT. In order to achieve the expected thermal advantages of the GaN-on-Diamond HEMT, the thermal resistance at the GaN/diamond interface needs to be kept as low as possible (i.e., <35m^{2}K/GW for 3X power). In strong contrast to the conventional high-temperature bonded GaN-on-Diamond wafer approach reported in [1], the diamond substrate in our device is attached to the GaN layer using a low-temperature bonding technology to greatly reduce the impact of GaN/diamond CTE mismatch. This also allows the GaN devices to be fully fabricated for very high yield before the diamond bonding, eliminating wafer bow related processing issues - due to GaN/diamond CTE mismatch - observed in conventional GaN-on-Diamond wafers

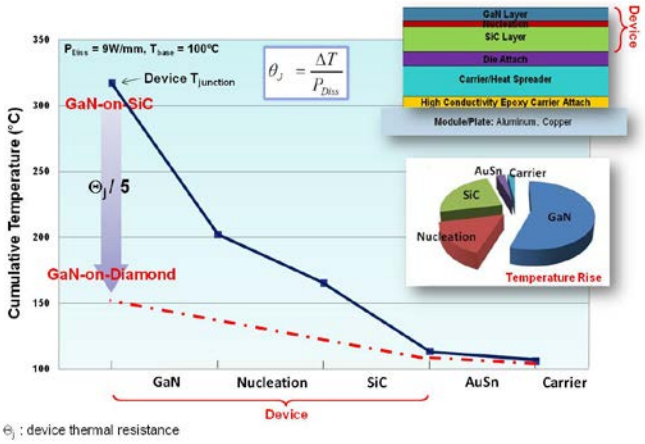

Figure 2. Conventional GaN-on-SiC HEMT device dominates temperature rise in power module stack up, affecting reliability, power and efficiency. An improvement in device thermal resistance with a high thermal conductivity substrate substantially lowers the temperature rise.

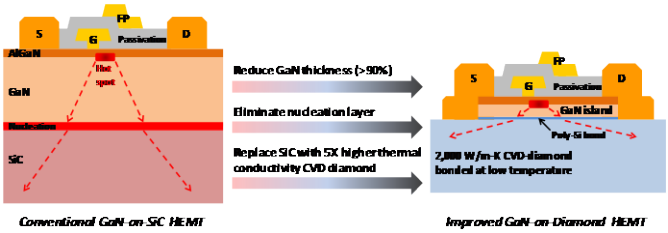

Figure 3. Next generation GaN-on-Diamond device structure provides ~40°C lower junction temperature and vast improvement in device power handling capability over the existing GaN-on-SiC HEMT.

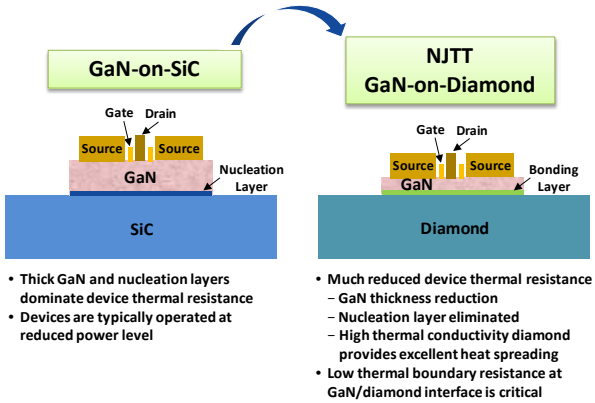

Figure 4. Comparison of a conventional GaN-on-SiC HEMT to the NJTT (DARPA Near Junction Thermal Transport) GaN-on-Diamond device. In order to achieve the expected thermal advantage of the GaN-on-Diamond HEMT, the device needs to have a very low thermal boundary resistance (TBR) at the GaN/diamond interface.

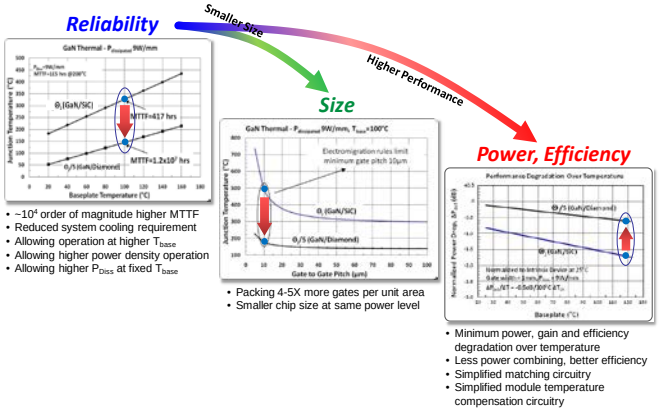

Figure 5. The new GaN-on-Diamond device technology enables wider trade space among reliability, size and performance for new capabilities in future military systems.

As mentioned above, using GaN-on-Diamond wafers, the GaN device can expect an increase in power handling capability as well as operating at higher baseplate temperatures, which would reduce system-level cooling requirements. As shown in Figure 5, since GaN-on-Diamond runs cooler, a significant improvement in device

reliability (~10,000X longer operating lifetime) is expected, which can be traded for smaller hardware size, increased transmit power and higher efficiency.

Design And Fabrication of GaN-on-Diamond HEMTs

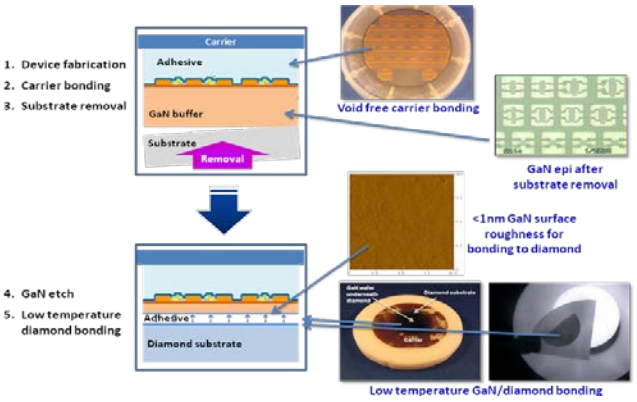

Figure 6. "Device first" GaN-on-Diamond (completing device processing before diamond bonding) process flow and achieved results at each step.

Figure 6 shows the "device first" wafer process flow and demonstrated technology at each processing step. The Si-based diamond bonding process, performed at room temperature, is fully compatible with the GaN wafer processing. The technical challenge in realizing this device technology remains in both carrier and diamond bonding areas. The ability to obtain uniform and very flat patterned GaN epi layer after the substrate removal (Si, sapphire or SiC) and to achieve a mechanically strong and uniform diamond bond with very low GaN/diamond thermal interface resistance are the keys to a successful demonstration of the device.

Since the device runs cooler, it is possible to reduce the device gate pitch to achieve higher output power while maintaining a similar junction temperature. As shown in Figure 7, with the reduction of gate pitch from 49µm to 10µm, the end result is a GaN-on-Diamond device with >5X improvement in power handling capability over GaN-on-SiC, together with uncompromised reliability that will enable higher power RF sources in smaller footprints, and major reductions in system SWaP due to associated relaxation of prime power and cooling requirements.

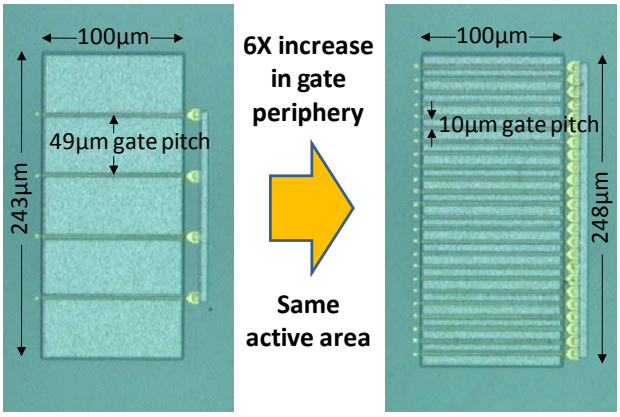

Figure 7. Photos of standard 4x100µm and small-gate-pitch 24x100µm GaN HEMTs having the same device area. With a diamond substrate, the device on the right has a 6X increase in gate periphery, and therefore will provide 5-6X more RF power than the standard GaN HEMT with a SiC substrate (while maintaining a similar junction temperature.)

Shown in Figure 8, with this approach, a GaN-on-Diamond HEMT with the diamond substrate bonded at room temperature has been fabricated. It should be noted that this device technology is also MMIC compatible and can be made on 4" or 6" diamond substrates (Figure 9).

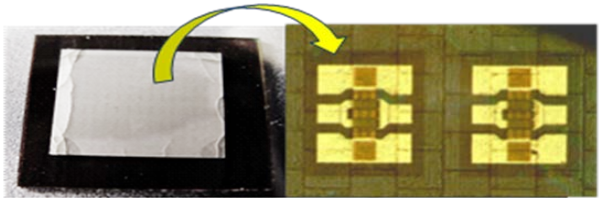

Figure 8. Demonstrated GaN-on-Diamond devices on a 1" square diamond substrate.

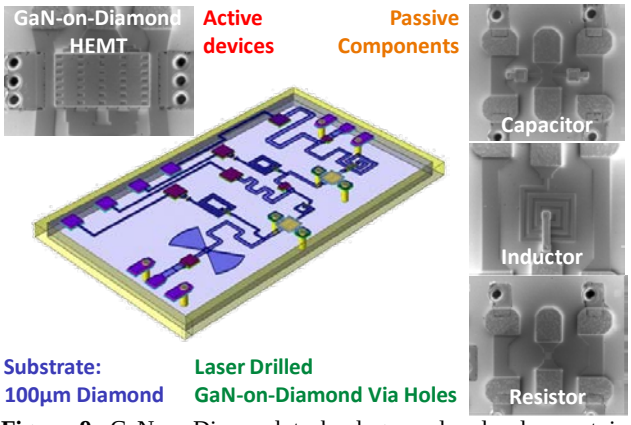

Figure 9. GaN-on-Diamond technology under development is MMIC compatible.

7
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COMPARISON TO OTHER THERMAL MANAGEMENT TECHNOLOGIES

Table I is a comparison of the GaN-on-Diamond approach with others we considered for chip-level thermal management. This approach achieves the best overall combination of high heat dissipation, ease of implementation and full MMIC compatibility. In contrast, approaches involving liquid micro-channels or convection cooling techniques, while capable of high heat dissipation, are much more difficult to realize in practice. Thermo-electric solutions utilizing the Peltier effect require significant additional DC power, lowering overall system efficiency.

TABLE I
COMPARISON OF PROPOSED GAN-ON-DIAMOND APPROACH VS OTHER METHODS FOR CHIP-LEVEL THERMAL MANAGEMENT

	Diamond Wafer Bonding "Our Approach"	Conventional GaN-on-Diamond	Microchannel Liquid Cooling	Thermo-Electric Cooling
Heat Dissipation Method	Conduction	Conduction	Conduction + physical transport	Peltier effect
Heat Dissipation Capacity	Excellent	Fair	Excellent	Fair
Additional Power Requirement	None	None	Some	High
Operational Temperature Range	Unlimited	Unlimited	Limited (upper boiling limit)	Unlimited
Difficulty of Implementation	Medium	High (CTE, wafer bow)	High	Medium
MMIC Compatibility	Yes	Yes	Difficult	Yes

POTENTIAL TECHNOLOGY INSERTIONS

GaN-on-Diamond is ideally suited to wideband EW amplifiers as they are the most thermally challenging – efficiencies are only half those of narrower bandwidth amplifiers used in radar or communications due to impedance-matching constraints, and these systems typically operate CW in tough environments, with high baseplate temperatures. Key system attributes are efficiency (maximizing effective radiated power for fixed prime power), reliability and weight. GaN-on-Diamond reduces channel temperature by ~40°C for the same operating conditions (P_{diss}). As seen in Table II, several BAE Systems wideband applications could benefit greatly from the enhanced thermal properties of the GaN-on-Diamond technology. For example, in one application we envision replacing three GaAs PHEMT chips in a power amplifier (PA) with one GaN-on-diamond HEMT chip, producing double the RF power, eliminating combiners, cutting cost and reducing module footprint area by 75%.

TABLE II
EXAMPLES OF WIDEBAND APPLICATIONS WHICH CAN BENEFIT FROM THE NEW GAN-ON-DIAMOND TECHNOLOGY

Application	Benefits of GaN-on-Diamond
Phased Arrays for Electronic Attack	Significant increase in system reliability, higher ERP, reduced chip size/cost
Solid-State Power Amplifier (SSPA)	Reduce size, cost and weight, convert higher efficiency into higher Pout for same DC power
High Power Tube (TWTA) Replacement	Lower life cycle cost, eliminates TWTA high voltage power supplies, increase reliability and power level vs. GaN-on-SiC SSPA
Wideband Communications	Reduces chip size, cost, amplifier size and weight, increase reliability

SUMMARY

GaN epi bulk thermal conductivity, interfaces and substrate material play a significant role in device temperature rise. The power performance of the GaN technology is projected to further improve by 3-5X, if current thermal bottlenecks at the transistor and MMIC level can be eliminated. With a well designed GaN-on-Diamond HEMT, one expects that the GaN device thermal resistance can be reduced by a factor of 5-10X, allowing the device to run significantly cooler and therefore more reliably and efficiently. Compared with current GaN-on-SiC technology, this new device will be more efficient and provide longer operating lifetime. The technology also enables a smaller chip size or much more power per unit chip area. GaN-on-Diamond is ideally suited to wideband EW PAs as they are the most thermally challenging.

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REFERENCE

[1] Wasserbauer, et. al., "Diamond cools high-power transistors," *Compound Semiconductor*, p.25, Nov. 2007.