SESSION 8b:
PROCESS – METAL

Chairs: Suzanne Combe, *TriQuint Semiconductor*
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At the heart of the CS ManTech is the sharing of advancements in process methods, tools, metrology, which is the outcome of thinking out-of-the-box and challenging conventional methods to achieve unique solutions. This is evident in this session for Process – Metals where we have five contributing papers; two are focused on frontside metallization and three are focused on backside metal and bump processes. We begin with a paper from Skyworks Solutions, which describes the transfer of Skyworks Solutions E-mode pHEMT technology to production and the application of an optical transmission technique to accurately characterize and match their critical gate metal deposition thickness on multiple e-beam evaporation systems. The second paper covers a novel lift-off approach developed by the Electronics Science and Technology Division of the Naval Research Laboratory (NRL) for selective patterning of material films deposited at high temperatures. NRL has circumvented the low temperature limitations of conventional photoresist methods by employing a bi-layer structure composed of silicon nitride (SiN) and germanium (Ge). NRL is exploring this novel inorganic lift-off approach for selective epilayer regrowth that will enable reduced contact resistances for GaN transistors. The third paper discusses demonstration of an electroless plating technique for palladium (Pd) with a crystalline adjuster. The authors are from the High Frequency & Optical Device Works group of Mitsubishi Electric Corporation. This technique enables an effective Pd diffusion barrier for backside copper (Cu) metallization on GaAs devices that is uniform and thermally stable. This work makes it possible to replace Au with the more cost-effective Cu for GaAs backside metallization. The fourth paper from TriQuint Semiconductor discusses a systematic approach they used to optimize their Cu bump process to address yield limiters identified during their production ramp-up. The authors review their work on optimizing their plating bath solution stability and plating bath hardware configurations, methods for operator training using videos, and implementation of 3-D automated optical inspection. We conclude the session with a paper from Freescale Semiconductor which discusses how they addressed challenges of transferring their GaAs RF power amplifier process to a different fab with different tool sets. The work presented in this paper focuses on issues the authors observed with die bond voiding in their PbSn die attach assembly. They describe how they optimized their backmetal process and discuss related findings.