SESSION 10b:
PROCESS – INTEGRATION
Chair: Steve Mahon, *Cascade Microtech, Inc.*

Device and process technology is all well and good but if it doesn't integrate into the environment or the system it has little chance of success. This session on Process Integration looks at a few perspectives of bringing all the elements together.

We lead off the session with a paper from Taiwan, where a team from WIN, the world's biggest GaAs foundry, describes layout practices for HBT circuits that can shrink die size and the performance tradeoffs involved in the various options. It is classic process and device layout integration to be used for getting more die and dollars out for every wafer.

Next, Skyworks reports an investigative look at the process and materials interaction on BiFET variation. The authors investigate FET geometry, using DOE, to flesh out the source of deviant FETs and its interaction with the process and material set.

The next two papers look outside the integrated circuit with filter elements and packaging technologies that provide the full integration that is driving our industry's growth. The filter group at TriQuint gives us an update on the tremendous progress in performance of Bulk Acoustic Wave (BAW) filters that is making it the preeminent filter technology for mobile devices. This paper will also present the advanced wafer-level-packaging (WLP) that allows BAW devices and CS devices to be compactly integrated. Dr. Karlheinz Bock looks further out on the possibility of the integration of our high frequency CS devices with flexible circuits and flexible interconnect. These low cost techniques open the window to even higher volume in the future.

We bring it all home with a paper that tackles the long-standing problem of hermetic coating of CS devices. An author at TriQuint uses finite element analysis to model the proper conditions for crack free nitride passivation – a classic problem.

This not-to-miss session is sure to have something for everyone!