Power Output of Multijunction Solar Cell Wafers

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Abstract

Power output of multijunction solar cell wafers is important for quantifying manufacturing costs in terms of dollars per watt and estimating the number of wafers needed for a project given in megawatts. Power output of wafers depends on a number of factors directly and indirectly related to cell size. In this paper we analyze the relation between cell size, efficiency, perimeter effects, temperature, and wafer area utilization. These guidelines can also be used to find the optimum cell size for a given application.

INTRODUCTION

In the last two decades concentrated photovoltaics (CPV) has rapidly advanced to become a feasible clean energy technology. The CPV technology uses multijunction solar cells with each junction designed to absorb from a separate portion of the solar energy spectrum, allowing for solar energy conversion with high efficiency. Currently Solar Junction Corporation holds the world record in cell efficiency with a 44.0% cell, which was verified by the National Renewable Energy Laboratory (NREL) [1]. The CPV roadmap targets 50% efficient cells in production by the end of the decade, which will push CPV system efficiencies above 40%.

CPV systems are often compared to flat-plate photovoltaics in a number of ways. Even though CPV is part of the solar industry at large, CPV manufacturing requirements are very different than those of flat-plate photovoltaics. The flat-plate photovoltaics industry often requires specialized manufacturing equipment whereas CPV cell manufacturing uses standard compound semiconductor processing tools routinely used in many foundries all over the world. In that sense a CPV cell manufacturing line is very similar to an LED manufacturing line.

In the greater solar industry it is customary to refer to manufacturing volume in terms of megawatts per year (MW/y) and manufacturing costs in terms of dollars per watt ($/W). Such quantification has been found to be convenient for comparison of flat panel photovoltaic cells in terms of manufacturing costs. CPV manufacturers are often asked to compare their cost-performance using the same metrics, which do not necessarily provide an accurate comparison due to major differences between the CPV and flat-plate technologies. Levelized Cost of Energy (LCOE) has been adopted as a more accurate assessment of overall financial performance of energy systems [2]. Nevertheless, MW/y and $/W metrics are widely used in the solar industry.

In the CPV industry manufacturing capacity is more conveniently expressed in terms of number of wafers and manufacturing costs are determined on a per-wafer basis. The power output of a CPV wafer is needed to estimate the corresponding MW/y and $/W values. However, for the CPV technology, even within the same technology base, the power output of a CPV wafer varies significantly based on the cell and module design preferences.

This paper investigates several factors impacting the power output of multijunction solar cell wafers for a given technology base. In the paper we first discuss the value of cell efficiency in CPV systems. Subsequently, we discuss the dependence of cell efficiency on cell size, cell perimeter effects, and temperature. We also discuss the impact of cell size, busbar size, and kerf on utilized active area per wafer. There is interdependency among the aforementioned factors, which determines how much power can be obtained per wafer. The power output of a multijunction solar cell wafer is important for manufacturing cost calculations in terms of $/W and also for LCOE calculations. The paper can also serve as a guideline for CPV system manufacturers when designing modules and help them choose an optimal cell size for a particular application.

VALUE OF CELL EFFICIENCY IN CPV

While cost is the single most important parameter for the competitiveness of photovoltaic systems, the cost structure is different in flat-plate and CPV systems. For flat-plate systems 67% of an average project's total cost was in the PV module in 2008. Such a high percentage of module cost has been driving a reduction in manufacturing costs and the percentage dropped to 50% in 2011 and 32% in 2012 [3]. While the flat-plate module costs dropped significantly from 2008 to 2012, average cell efficiency in production has not changed much.

On the other hand, in a typical CPV system the cost of the cell is about 10% - 20% of the overall installed system cost. Increasing cell efficiency is one of the main drivers of overall system cost reduction for the CPV industry because it is leveraged across every component in the entire CPV

system. For example, for a base cell efficiency of 40%, an absolute increase of 2% in cell efficiency increases the power output of the cell by 5%. Hence, for a given installation size in megawatts, using cells with 2% higher efficiency directly results in 5% fewer panels that need to be installed, which in turn means 5% fewer poles in the ground, 5% fewer tracker systems, 5% less land, and 5% lower operations and maintenance costs. According to one analysis [4], increase in cell efficiency will contribute about 25% of the projected cost reduction in CPV systems from 2011 to 2020. As a comparison, contribution from the decrease in cell manufacturing costs is expected to be only 4% in the same period.

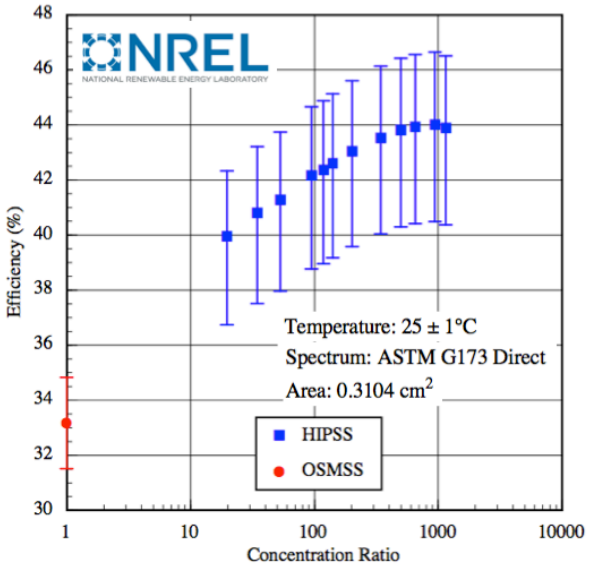

Fig. 1: Efficiency vs. concentration characteristics of Solar Junction's world record cell: 44.0% efficiency under 947 suns.

Solar Junction's Cell Technology

Solar Junction is currently manufacturing multijunction solar cells made of InGaP / GaAs / GaInNAsSb subcells grown lattice-matched on gallium arsenide substrates. The bandgaps for the top, middle, and bottom subcells are 1.88 eV, 1.42 eV, and 1.0 eV, respectively, allowing for an optimal partitioning of the solar spectrum for the highest efficiency. Recently, Solar Junction's 5.5 mm x 5.5 mm cell achieved a world record with 44.0% power conversion efficiency under a concentration of 947 suns (verified by NREL). The previous record was also set by Solar Junction with 43.5% efficiency in 2011 [1]. Solar Junction's cells are on a lattice-matched platform, allowing for a realistic roadmap towards 50% efficiency by 2017.

Fig. 1 shows the efficiency vs. concentration profile of the world-record cell as measured by NREL. The concentration where the efficiency peaks is important for practical applicability of solar cells. The world record efficiency was measured at 946 suns, which is aligned with the trend in the CPV industry towards higher concentrations in the neighborhood of 1000 suns.

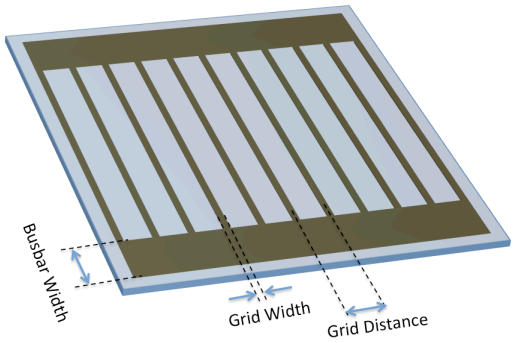

Fig. 2: Schematic of a multijunction solar cell

Cell Size and Performance

In the CPV industry, cell sizes range from submillimeter dimensions [5] to about 1 cm x 1 cm [6]. The 'right' cell size depends on the particular application. In this section we will analyze factors impacting performance that depend on cell size directly or indirectly.

Cell Design

For a given epitaxial design an optimization is done on a number of design parameters in order to achieve the maximum efficiency possible. Fig. 2 shows the schematic of a typical multijunction solar cell with two busbars. In such a cell there is trade-off between grid shadowing and resistive losses in the emitter (top subcell) and along the gridlines. While the busbars are not part of the active area and hence do not result in shadowing loss, they affect utilized area per wafer.

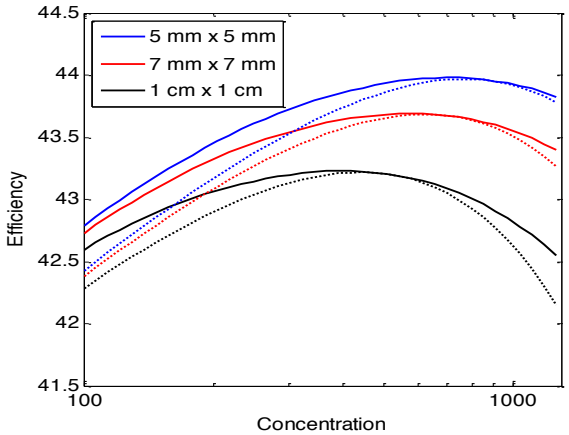

Fig. 3 Simulated efficiency as a function of concentration for different cell sizes. Solid lines show device optimized for each concentration and dashed lines show results for constant grid spacing.

Fig. 3 shows efficiency as a function of concentration for cells with different aperture areas. The dashed curves show the change in efficiency for constant grid spacing. The solid curves show the case for which the grid distance is optimized for best possible performance for each concentration. Even with optimized grid spacing, the

efficiency drops at higher concentrations due to increased I^2R losses. Fig. 4 shows how the efficiency changes as a function of cell size for three different concentrations. The drop in efficiency with increasing cell size is due to increased I^2R loss resulting from longer gridlines.

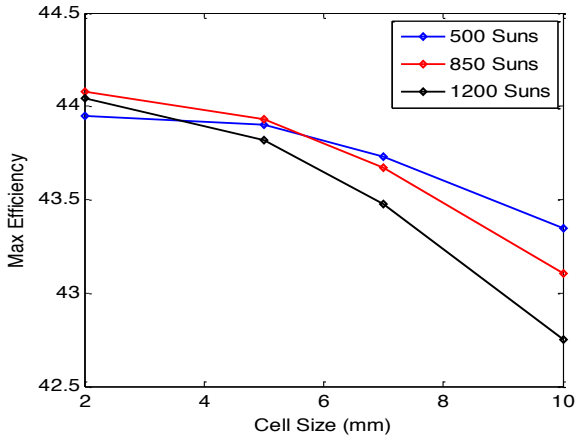

Fig. 4 Simulated efficiency as a function of cell size at concentrations of 500, 800, and 1200 Suns.

Perimeter Effects

In GaAs-based solar cells, perimeter recombination is known to have a non-negligible impact on performance, especially for small cells under low concentrations [7]. The simulation in Fig. 4 also incorporates perimeter recombination effects: As the cell size becomes smaller, and hence the perimeter-to-area ratio becomes larger, the increasing trend in efficiency tails off and reaches a plateau. The perimeter effect is more dominant for the 500 Suns case compared to the other two cases. Fig. 5 shows open circuit voltage (V_{OC}) data obtained under concentrated light for different cell sizes. V_{OC} shows a steeper decrease for cell sizes smaller than 3 mm x 3 mm, suggesting that the impact of perimeter recombination is more significant in that cell size range. An effective technology for sidewall passivation will be instrumental in mitigating the impact of perimeter recombination.

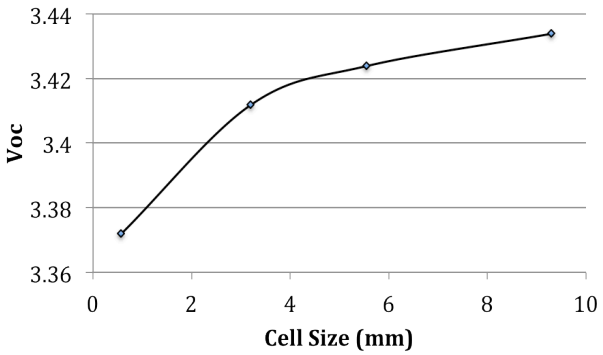

Fig. 5. Open circuit voltage change as a function of cell size.

OTHER FACTORS IMPACTING THE PERFORMANCE

Temperature

During normal operation under concentrated sunlight multijunction solar cells are at elevated temperatures, typically ranging from 20 °C – 60 °C above ambient. Temperature increase redshifts the bandgaps of the subcells, reducing the V_{OC} and shifting the spectral response (quantum efficiency) of the cell. The shift in quantum efficiency changes the current output of the cell and the current balancing among the subcells, which changes the fill factor. In addition, metal resistivity and certain other cell parameters also depend on temperature. As a result, the efficiency degrades by about 0.03% - 0.08% absolute efficiency per °C [8].

Operating temperature depends on cell size and receiver design. Generally, it is easier to remove heat from smaller cells, often without sophisticated heatsink designs. On the other hand, larger cells typically operate at much higher temperatures. Moreover, the temperature is typically higher in central locations, creating a spatial change in the spectral response across the cell, which may result in additional series resistance loss.

Spectral Transfer Function

Spectral transfer function (STF) of the optics used in a CPV system can have a significant impact on the performance. For example, acrylic lenses have characteristic absorption regions in the ultraviolet and in the infrared (IR). Therefore, a multijunction solar cell that has a current matched design for optimum performance under unity transmission (e.g. laboratory test conditions) may be current-limited by the lower subcell in a CPV module with acrylic lens due to IR absorption. Such a change in current balancing can reduce the current output of the cell and impact the fill factor.

Nonuniform Illumination and Chromatic Aberration

In some system designs beam intensity may be highly localized near the center of the cell. Hence, the concentration changes spatially, resulting in increased series resistance losses. Furthermore, each subcell may be seeing a different spatial distribution of intensity due to chromatic aberration, resulting in additional series resistance losses.

WAFER AREA UTILIZATION

Wafer packing density directly impacts the power output of multijunction solar cell wafers. In general, wafer area can be filled more effectively with smaller chips. However, as the cell size gets smaller, busbars and dicing streets take up a larger percentage of the chip area, since they do not scale with the cell size. Utilized Active Area (UAA) of a wafer is defined as the active area of a cell (region between the busbars) times the number of cells obtained from that wafer. UAA can be expressed as percentage of the total area of the

wafer. Fig. 6 shows the UAA as a function of cell size for 4-inch and 6-inch wafers, for cells with 100 µm and 200 µm busbars, with the assumption of 3 mm exclusion zone and 50 µm dicing streets between cells. 6-inch wafers offer better area utilization for cell sizes above ~ 2 mm x 2 mm. As of today multijunction solar cell manufacturers are typically on a four-inch line. Moving to six-inch wafers will offer larger active area utilized per wafer.

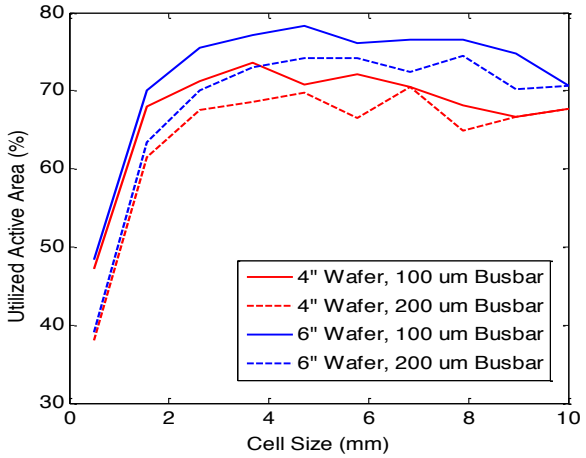

Fig. 6: Percentage of utilized active area on a wafer. (Assumptions: 3 mm edge exclusion and 50 µm dicing lane)

Power Output of Wafers

In practice, power output of wafers is a combination of all the factors discussed in this paper. Table 1 compares a few different cases in terms of the number of wafers needed for a CPV installation of 10 Megawatts, assuming unity transmission and uniform illumination under direct normal irradiance of 900 W/m^2. As seen, the number of wafers can vary significantly depending on the particular cell and system design parameters.

TABLE I
NUMBER OF WAFERS NEEDED FOR A 10 MW CPV INSTALLATION

Cell Size	Busbar Size	Conc.	Temp.	Wafer Size	# of Wafers
2 mm	100 µm	500 X	25 °C	4 inch	9,560
2 mm	200 µm	500 X	25 °C	4 inch	10,330
5 mm	200 µm	500 X	25 °C	4 inch	9,600
5 mm	200 µm	900 X	25 °C	4 inch	5,330
5 mm	200 µm	900 X	50 °C	4 inch	5,470
5 mm	200 µm	900 X	50 °C	6 inch	2,200
10 mm	200 µm	500 X	50 °C	6 inch	4,220
10 mm	200 µm	900 X	50 °C	6 inch	2,360

Conclusions

Power output of multijunction solar cell wafers depends on a number of factors directly or indirectly related to cell size:

1) Efficiency decreases with increasing cell size as a result of increased resistive losses on gridlines. On the other hand, as cells get smaller, perimeter effects impact the performance negatively. Therefore, especially for small cells, an effective sidewall passivation technique can boost the performance.
2) Larger cells typically have higher operating temperatures, which can result in lower performance. Receiver designs for large cells can benefit from sophisticated heatsink designs. Smaller cells can be advantageous in terms of thermal management.
3) System-level design parameters, such as spectral transfer function and nonuniform illumination also impact the power output of cells.
4) Wafer area utilization suffers from increased percentage of busbar and kerf on the chip for cell sizes smaller than ~ 2 mm x 2mm. Wafer area utilization decreases with increasing cell size due to the lost area from the edge die. 6-inch wafers in general provide better packing density than 4-inch wafers.

There are other parameters impacting cost that are proportional to the number of cells. Since large cells have low per-wafer counts, they typically have lower assembly costs. For cells smaller than ~ 2 mm x 2 mm assembly and testing costs can be significant.

The discussion given in this paper provides guidelines for estimating the power output of multijunction solar cell wafers. The guidelines provided can also be used by CPV system designers when they evaluate different cell sizes. The 'right' cell size for a given application will depend on the system design parameters of that application in addition to the general guidelines provided in this paper.

Acknowledgements

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