TransImpedance Amplifiers – what's the buzz?

The explosion in consumer demand for mobile electronics – and the global and seamless connectivity of those devices – is having the ancillary effect of driving the market for TransImpedance Amplifiers (TIAs). There are 6 billion cell phone in use today; 1 billion of these are "smartphones". An incremental 1.6 billion (with a "b") smartphones are sold annually. This is driving incremental investment in backhaul and cell tower infrastructure.

The emergence of the "Internet of Things", the reality of connectivity among devices that is seamless and transcends human interaction, is driving significant traffic to the broadband network. This is driving the demand for TIAs. The global market for optical amplifiers was $900 million in 2012 and anticipated to reach $2.8B by 2019. This 15% CAGR over an eight-year period makes this an important market to watch.

The relevant standards (IEEE 802.3ba) indicate that 4x25 Gbps or 10X10 Gbps parallel communications will be used to reach the 100 Gbps data rates that will be demanded to keep up with this surge. However, inherent cross talk between channels and higher power consumption conspire to degrade the power performance of these devices. Reducing the number of channels requires higher bandwidth TIAs.

Several companies are developing 100 Gbps TIAs (Inphi, Mindspeed, and others). They are utilizing 28X4 Gbps to reach the requisite bandwidth. But, the drive to increase bandwidth density will drive towards smaller form-factor, pluggable modules and small form factor on-board optical engines. These solutions are required to "future proof" the infrastructure investment.

Because of the high bandwidth requirements, TIAs have traditionally been fabricated utilizing III-V compound semiconductor processes. However, emergent advances in CMOS are proving promising also for TIA production. Among these bandwidth improvements in CMOS are a low power push-pull TIA (a PMOS transistor replaces the resistive load of common source in the TAI and the gate of the NMOS and PMOS are tied); other methods are being pursued.

This paper will pursue the various approaches to achievement of high bandwidth TIAs as well as the methods for on wafer measurement of these devices.