Yield Enhancement of 0.25 μm GaN HEMT Foundry Technology

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Abstract

A variety of process developments on the gate module and design optimization on the EPI structure where performed to support yield enhancement of 0.25μm GaN HEMT technology. The technological developments to be discussed pertain to the results of a gate pre-treatment DOE experiment, to implement the best condition for reliability improvement; a gate module process flow optimization, to minimize DC FET parameter variation; and the optimization of EPI buffer conditions, to stabilize the PCM performance and enable larger voltage rating. The developmental challenges will be elucidated followed by data showing the trade-off with reliability performance, stability and control of the critical parameters for high-yield production purposes.

The DOE plan of the gate pre-treatment is shown in Table 1. Four conditions with different combinations of pre-treatment approaches were implemented. The gate interface state was evaluated by pulsed IV measurement as shown in Fig.1. The DOE4 condition showed a relatively lower drain current degradation and also a larger capacitance as shown in Fig.2. The C-V measurement result revealed that different interfaces are formed for different pre-treatment conditions. The interface is observed by HAADF STEM imaging. An extra interface layer was observed for DOE1 but not in DOE4. Since the gate interface is quite critical to reliability test, DC-HTOL test is a good method to check the interface quality. A very significant difference in the DC-HTOL tests for the DOE conditions was observed as shown in Fig.4. The transistors were stress at peak junction temperature of 250C with 28V drain bias. It is very obvious that the DOE4 condition showed less drain current degradation and this was correlated to the gate pulse and C-V measurement results. For further evaluation of the repeatability and performance of this DOE4 condition, we choose another 20 dies for test till 500hrs and the result was promising.

After running prototype production volume with DOE4 pre-treatment condition, the variation of gate leakage and breakdown voltage was identified as the major yield killers. In order to improve the line stability, we found the root cause for the yield issue was a narrow process window of photo-resist coverage after gate metal formation as shown in Fig.5. The abnormal PR coverage profile was caused by un-certain and varying ohmic edge profile. Thus we implement the 2nd SiN first deposition process with the intent to enlarge the process window. The WAT trend chart showed a very promising result after this process change was implemented as shown in Fig.6. This process change also enabled an improvement in Vto shift and Gm swing with changing drain bias from 10V to 50V as shown in Fig.7. 10GHz pulsed load-pull at Vd=28V was measured for a 1.25mm transistor. The result showed that the process technology could realize transistors with P.A.E. above 50% and with output power density of 4.8W/mm.

Finally, we have an EPI buffer DOE design to get high ruggedness performance and voltage rating. The improvement in gate leakage and breakdown stability was shown in Fig.9. It's obvious that buffer condition 2 showed a more stable breakdown performance in terms of the compliance voltage at 160V. This new buffer design enables operating bias to be up to 50V and has applicability in future base-station applications and products.

Table 1

Split	Pre-treatment
DOE1	B1+B2
DOE2	B1
DOE3	B1+C1+B1
DOE4	B1+C1+B2

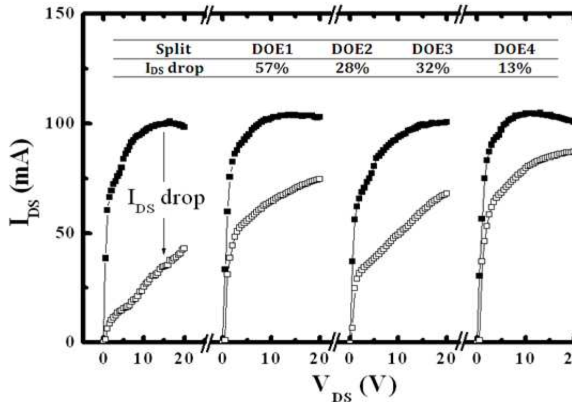


Fig.1 Gate pulse measurement for different pre-treatment conditions

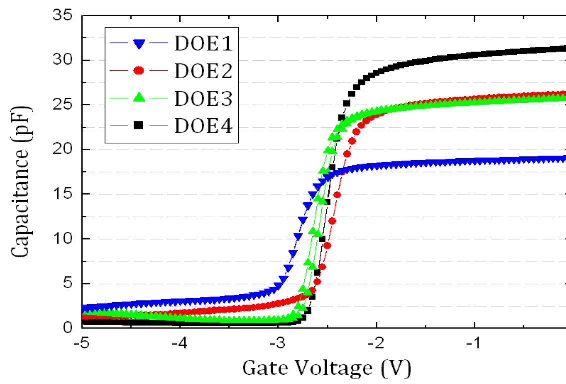


Fig.2 C-V measurement for different pre-treatment condition (@ 1MHz)

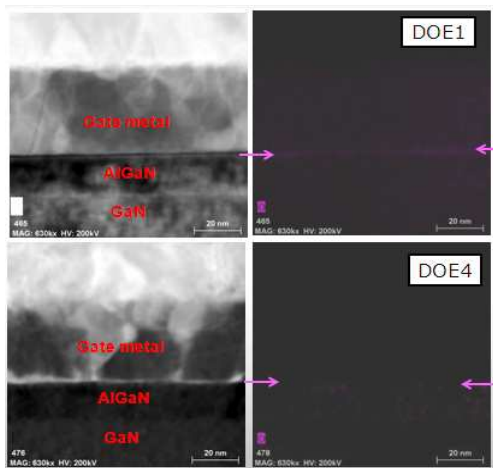
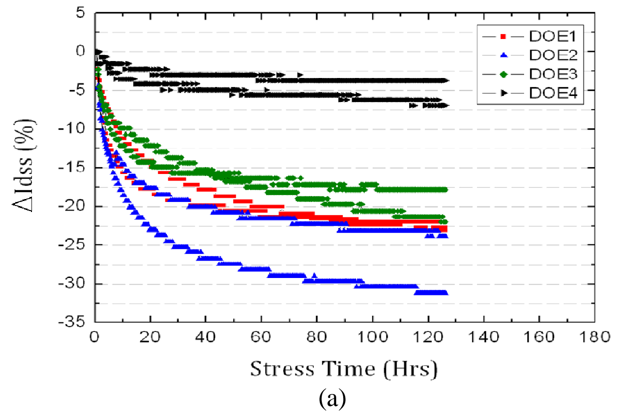
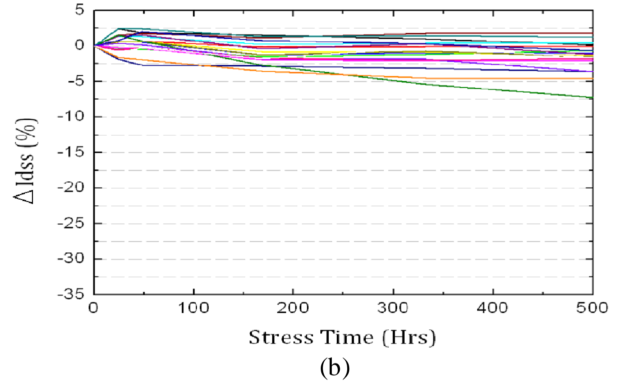


Fig.3 HAADF STEM image of gate interface for DOE1 and DOE4

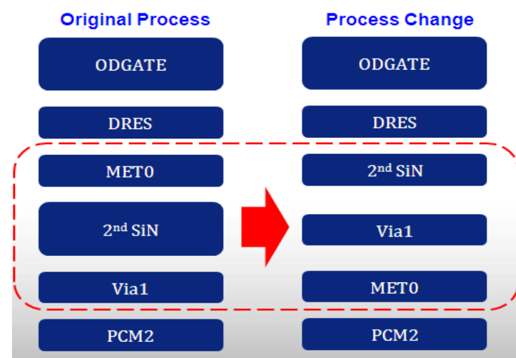


(a)

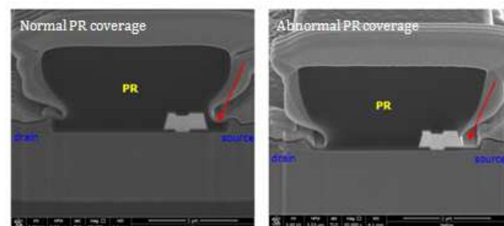


(b)

Fig.4 DC-HTOL test of (a) different DOE conditions, and (b) DOE4 condition with 20 dies. 28V drain bias and Tj=250C

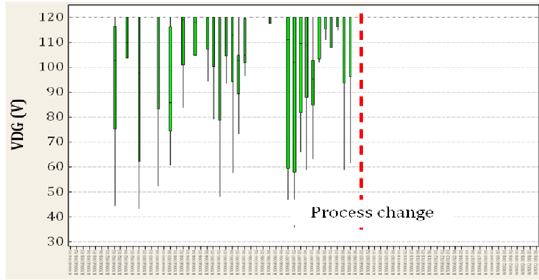


(a)

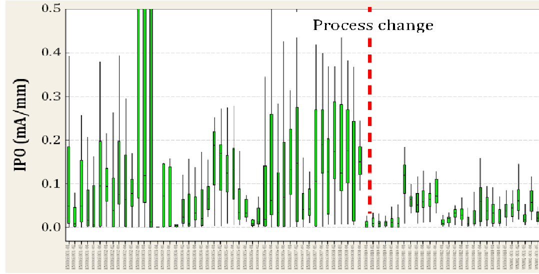


(b)

Fig.5 (a) Process flow comparison before and after optimization, (b) SEM image of normal and abnormal photo-resistance coverage

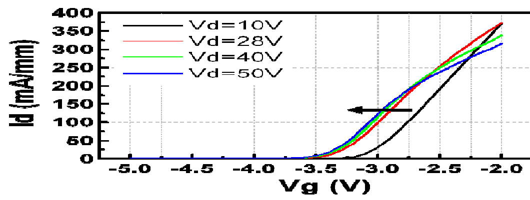


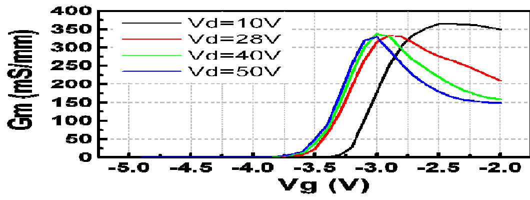
(a)



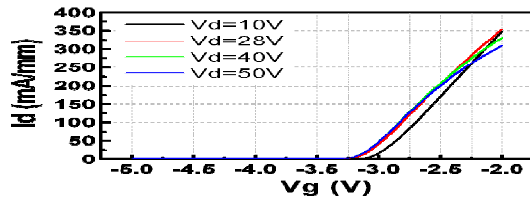
(b)

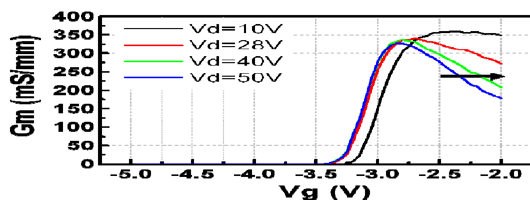
Fig.6 PCM trend chart comparison of (a) breakdown voltage, and (b) gate leakage current biased @ Vd=10V and Vg=-5V





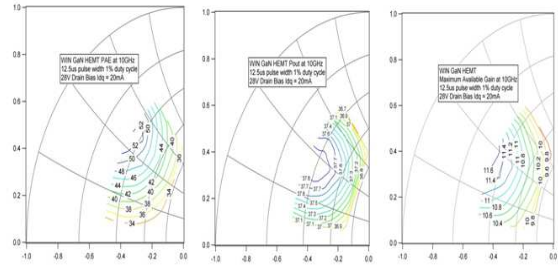
(a)





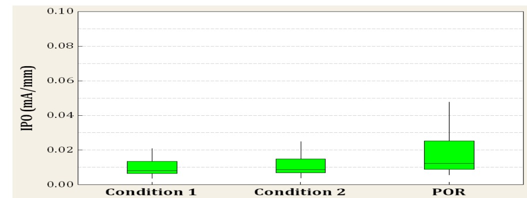
(b)

Fig.7 Transfer curve comparison of (a) original process flow and (b) after process change

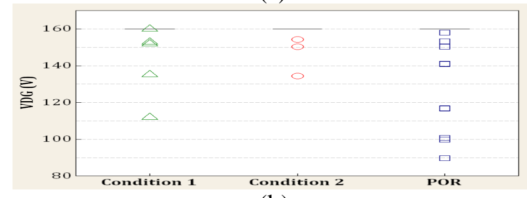


UGW (mm)	Frequency (GHz)	Linear Gain (dB)	P.A.E. @ max (%)	Pout @ max (dBm)	Pout @ max (Watt/mm)
1.25	10	11.6	52	37.8	4.8

Fig.8 Pulse load-pull performance @ 10GHz with pulse width=12.5 μ sec, duty cycle=1%. 28V drain bias and Idq=20mA.



(a)



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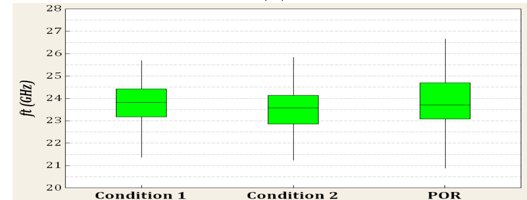
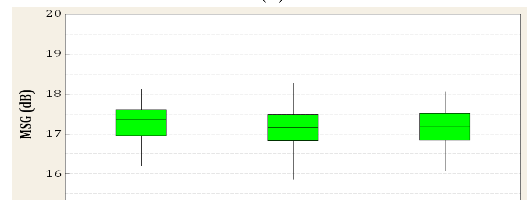


(c)



(d)

Fig.9 RF PCM performance of (a) gate leakage (IPO), (b) breakdown voltage (VDG), (c) cut-off frequency (ft), and (d) maximum stable gain (MSG) @ Vd=28V with different EPI buffer layer design.