An Optical 150-nm Y-Gate Process for InAlN/GaN HEMTs
Hiroyuki Ichikawa, Isao Makabe, Yasunori Tateno, Ken Nakata and Kazutaka Inoue
Transmission Devices R&D Laboratories, Sumitomo Electric Industries, Ltd.
1 Taya-chou, Sakae-ku, Yokohama 244-8588, Japan
Phone. +81-45-853-7318, Fax. +81-45-852-2913, E-mail ichikawa-hiroyuki@sei.co.jp

Abstract
An optical 150-nm-gate-length Y-gate process was successfully developed for InAlN/GaN high-electron mobility transistors (HEMTs). This simple process is suitable for low cost production. With this process technology, we could obtain a high transconductance of 460 mS/mm and a high current gain cutoff frequency $f_T$ of 70 GHz for InAlN/GaN HEMTs on high-resistance silicon substrates.

1. Introduction
Recently, high-speed operations of a current gain cutoff frequency $f_T$ more than 200 GHz have been reported for InAlN/GaN HEMTs with a gate length $L_g$ less than 100 nm [1–3]. However, complicated processes e.g., an electron beam lithography and a regrowth technology were necessary. Therefore, we focused on low cost and simple technologies suitable for mass production. We first used a high-resistance silicon substrate; it is more cost-effective than a semi-insulating SiC substrate. Secondary, we developed a Y-gate process without using an electron beam lithography. We used a conventional i-line stepper. This process enables us to obtain short $L_g$ of 150 nm and low parasitic gate capacitance.

In this paper, we describe the details of the device fabrication process. Then, we show DC and RF characteristics of InAlN/GaN HEMTs.

2. Device Fabrication Process
InAlN/GaN HEMTs epitaxial layers were grown by metal-organic chemical vapor deposition on 100 mm high-resistance silicon substrates. The typical structure consists of an AlGaN buffer layer, a GaN buffer layer, an AlN interlayer, a nearly lattice-matched InAlN barrier layer and a GaN cap layer. Sheet resistance is approximately 500 $\Omega$/sq.

An optical Y-gate process flow is shown in Fig. 1. First of all, a silicon nitride (SiN) film was deposited on the surface by sputtering using an electron cyclotron resonance plasma (Fig. 1(a)). This deposition method can create denser films than those of conventional plasma-enhanced chemical vapor deposition. The reflective index and the thickness of the SiN film were 2.02 and 40 nm, respectively. Then, a resist pattern with 1.0-μm-thick and 250-nm-width was obtained by an i-line stepper (Fig. 1(b)). In order to obtain the precise gate length, the shape of the resist pattern shall be as square as possible. The pattern was shrunk by O$_2$ plasma etching and reformed to the dummy gate with 100-nm-length (Fig. 1(c)). Then 300-nm-thick SiO$_2$ film was deposited on the pattern by a collimated sputtering (Fig. 1(d)). The SiO$_2$ film adhering to the sidewall of the resist was removed by a BHF solution (Fig. 1(e)). After lifting-off the dummy gate (Fig. 1(f)), SiO$_2$ of the ohmic region was etched by a combination of Cl$_2$/BCl$_3$ reactive ion etching (RIE) and a buffered hydrofluoric acid (BHF) solution (Fig. 1(g)). Since an etching ratio of SiO$_2$ to SiN by a BHF solution is approximately 100, etching is stopped at the SiN surface. The SiN film and the GaN cap layer were etched by CF$_4$-RIE and Cl$_2$/BCl$_3$-RIE, respectively (Fig. 1(h)). Source and drain electrodes were formed on the InAlN barrier layer by a conventional lift-off technique (Fig. 1(i)). Then, ohmic anneal was performed by a rapid thermal annealing. Next, the SiN film on the gate was etched by CF$_4$-RIE with SiO$_2$ mask (Fig. 1(j)). Finally, a gate electrode was formed on the GaN cap layer, and was lifted off by a conventional technique (Fig. 1(k)).

![Fig. 1 Y-gate process flow](image-url)
A transmission electron micrograph (TEM) image of the cross section of the InAlN/GaN HEMT is shown in Fig. 2. The source-gate distance \( L_{sg} \) and gate-drain distance \( L_{gd} \) were 150 nm, 1.0 \( \mu \)m and 1.3 \( \mu \)m, respectively. The gate sidewall was tapered and its angle was approximately 60º. We can control this angle by changing the SiO\(_2\)-thickness and RIE conditions. The angle is very important, since it determines the parasitic gate capacitance and the electric field at the gate edge. We optimized this angle with the calculation by the device simulator.

### 3. DC and RF Characteristics

We measured the DC characteristics of the InAlN/GaN HEMT. The \( I-V \) curves are shown in Fig. 3. Figure 3(a) indicates the drain current \( I_d \) and the drain voltage \( V_d \) curves of the InAlN HEMT with \( L_g \) of 150 nm and the gate width \( W_g \) of 40 \( \times \) 2 \( \mu \)m. The gate voltage \( V_g \) was swept from -2 to 2 V with 0.4-V-step. Maximum current of 900 mA/mm was obtained. The on-resistance \( R_{on} \) extracted at \( V_d = 2 \) V and \( V_g \) in the range between 0 and 1.0 V was 1.8 \( \Omega \)mm. Figure 3(b) indicates transconductance \( g_m \), \( I_d-V_g \) and the gate current \( I_g-V_g \) curves at \( V_d = 10 \) V. Even if an InAlN barrier layer was used, low \( I_g \) less than 1 \( \times \) 10\(^{-5}\) A/mm was obtained due to introduction of the GaN cap layer. Good pinch-off characteristics were observed while \( L_g \) is as short as 150 nm. The peak \( g_m \) of 460 mS/mm was achieved.

Figure 4 shows the RF characteristics. We measured the \( S \)-parameters using an Agilent 8510C network analyzer for the InAlN/GaN HEMT with \( L_g \) of 150 nm and \( W_g \) of 50 \( \times \) 2 \( \mu \)m from 10 to 80 GHz. After the pad parasitic was de-embedded, \( f_t \) of 70 GHz and maximum oscillation frequency \( f_{max} \) of 150 GHz were obtained under the bias condition of \( V_d = 10 \) V and \( I_d = 150 \) mA/mm. We also extracted gate capacitance \( C_{gs} \) from an equivalent circuit model obtained from the measured \( S \)-parameters. \( C_{gs} \) of the InAlN/GaN HEMT with Y_gate was reduced by half than that with T-Gate at the same \( L_g \). Therefore, we confirmed that the Y-gate process is effective for reduction in parasitic \( C_{gs} \).

(All the characteristics including \( C_{gs} \) would be described in the final paper)

### 4. Conclusions

We demonstrated an optical Y-gate process for InAlN/GaN HEMTs on high-resistance silicon substrates. This process enables us to obtain short \( L_g \) of 150 nm and \( C_{gs} \) reduction. As a result, high-speed operation of \( f_t \) 70 GHz was successfully achieved. This simple process is suitable for low cost and high performance fabrications.

### References