Yield Improvement of Voltage Regulator in Next-Generation Wifi Front-End Module

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ABSTRACT

During a recent period, the RFMD Wireless Connectivity group experienced a series of yield problems with their Wifi products line. Through detailed data analysis at the process, device, circuit, and package level, a number of yield limiting factors were uncovered and steps were taken to reduce the yield loss. This paper seeks to document the productive events that took place as well as what we have learned, technical and institutional. We believe this learning can have an impact on the overall GaAs semiconductor community.

The framework of this paper is based upon the data analysis presented in [1]; it is through automatic assembly of "Big data" taken from various stages of wafer fabrication, packaging and assembly, and leveraging the data exploration capability of the Universal Data Query software to find the starting point for detailed analysis. Going further to find the root cause, we reviewed datasheets, delved into IEEE journals, simulated circuits in ADS, updated device-level models, and then conducted numerous meetings with different teams within and outside of the company. As many have articulated the yield improvement process in general terms [2][3][1], we will use this particular experience as a case study, to highlight the various challenges we have encountered at various stages. The outline of this paper is as follows:

1) timeline of events that took place.
2) actions taken by the various departments including wafer fab, epi vendor, and product line, as well as interactions between different groups(Section III).
3) recommendations for future improvement.

From the technical side, we found that Wifi products are failing for idle Icc, TX Pout, and EVM. Using the UDQ [1] to examine packaged, KGD, PCM, and epi data, we accurately pinpointed the failure to be the regulator circuit, and determined that Vreg was sensitive to the transconductance variation of the pHEMT device. We were able to precisely correlate Gm variation to epi growth details, and even trace its origin the circuit-level. Yield improvement can be categorized into the following stages:

1. control the yield failure at packaged test by tightening KGD and PCM specs
2. implement a temporary adjustment with epi control
3. permanently change the epi growth procedure
4. improve the PDK model to include process variation
5. solve the root cause by changing the circuit design.

Each of these aspects will be discussed in detail, without disclosing propriety information. By examining the formal interactions between wafer fab, product line, epi vendors, PDK modelers, and circuit designers, we have identified several key points which enabled yield improvement in every stage, and we further recommend ways to improve/encourage dialogue between different groups to prevent problems like this from happening in the future.

TIMELINE OF EVENTS THAT TOOK PLACE

Day 1: Product line reported to the fab yield team they were experiencing yield loss on several wifi FEMs, mainly due to EVM problems. Product line wanted to find out if the yield loss was due to any changes from wafer fab. Regular meetings were set up to improve and encourage dialog between various product groups and the Fab.

Day 4: The yield engineer responsible for the pHEMT technology quickly used the UDQ to find commonality between package, KGD, PCM, epi, and tool data. Details of this data analysis will be discussed in full paper; the result is summarized in Figure 1, showing that the packaged test level EVM is correlated to pHEMT voltage regulator measured during KGD (circuit level), which in turn is correlated to the device-level Gm. The pHEMT's performance could affect EVM either through the RF switch or the voltage regulator for the HBT PA. Since the regulator voltage is very critical to the PA function, a tighter Vreg spec limit was set to improve packaged test yield.

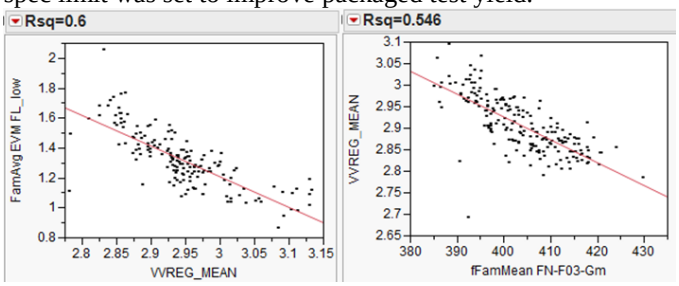

Figure 1. Correlation of package, KGD, PCM using UDQ

Day 12: The anomalous variation of Gm was traced to a specifc reactor material. The impact of Gm variation by on the rogue material was communicated to epi vendor, and the vendor representatives became actively involved to understand what had happened. For the time being, epi material from that reactor was blocked from being kitted into lots. Once this short-term fix was in place, we shifted our focus to a long-term solution, which will be described below.

YIELD IMPROVEMENT FROM EPI CONTROL

Monitoring PCM data is critical to the epi-growth process. By monitoring look-ahead wafers in a growth campaign, the epi vendor makes adjustment to the growth process to make sure wafers are meeting PCM targets. Since pHEMT technologies were originally used as RF switches, epi growers and yield engineers were mostly focused on parameters relevant for that application; namely leakage current, Vpo, and Idmax. More analog-oriented parameters such as Gm were less important. In some situations, an adjustment to make Vpo and Idmax on-target resulted in making Gm off-target.

The link between Gm and epi growth became very clear after a series of meetings internally as well as with epi growth engineers. Various past DOE lots and previous excursions were reviewed, as well as recent epi data. The DOEs provided epi vendor critical info for them to control their growth process.

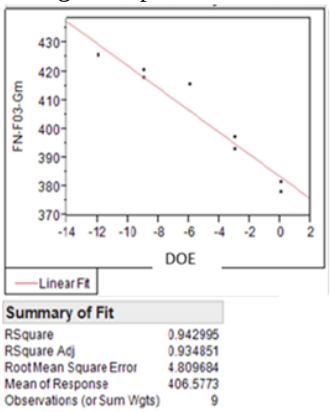

Figure 2. pHEMT Gm sensitivity observed in a DOE.

DEVICE MODELING

Ideally the process variation of a technology should be accurately reflected in the model, such that designers can simulate how the process variation will impact production circuits. In effect an inaccurate model increases the liability of the fab to final yield loss. Usually Monte Carlo process models are in place by the beta stage of the technology development. However it seems that the pHEMT model in particular is lacking in many aspects, and the recent development on pHEMT model is summarized below.

The most effective way of measuring model accuracy would be to simulate the entire PCM test, and benchmark against actual PCM data. If the fab is concerned about variation of certain parameters (ie Vpo or BVgdo) to measure them and place spec limits on them, they need to be reflected in the model. About some 20 PCM parameters were simulated simultaneously and compared against actual data.

To compare simulation and actual PCM data, individual pHEMT site data were collected through the UDQ. A JMP script was writen to convert PCM JMP tables into a ADS readable format, so that simulation and PCM data could be plotted together.

During this exercise, the D-mode FET model was found to be off-target. This discrepancy in the D-mode FET model was reported to the modeling team. After several iterations of retuning and examining the model against PCM data, the improved D-mode FET model was demonstrated to be quite close to the hardware. For the sake of brevity Figure 3 shows the final result of the D-mode FET Monte Carlo models. The models are not only on-target with PCM data but also well-captures the production circuit data, giving deeper insight into the circuit itself. It will be shown in more detail in the full paper.

Reference:

[1] P. Carroll *et al.*, 2012 CSMANTECH Tech. Dig., May 2012

[2] Eastham *et al.*, 2012 CSMANTECH Tech. Dig., May 2012

[3] Roesch *et al.*, 2012 CSMANTECH Tech. Dig., May 2012

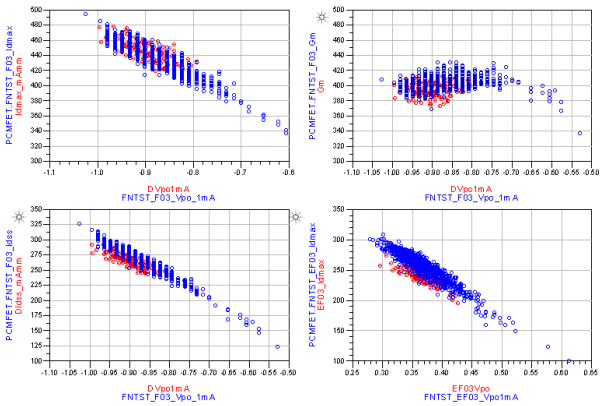

Figure 3. Updated pHEMT model; red (data), blue (model)