

## **Effects of Field Plate and Epitaxial Wafer on AlGaN/GaN HEMTs with Active Harmonic Tuning**

Keiichi Matsushita, Hiroyuki Sakurai, Akio Miyao, Yukio Takahashi, Kazutaka Takagi

Microwave Solid-state Department Toshiba Corp.

1, Komukai Toshiba-cho, Saiwai-ku, Kawasaki, 212-8581, Japan

Phone +81-44-549-5282, Fax +81-44-548-5955, e-mail: keiichi.matsushita@toshiba.co.jp

### **Introduction**

AlGaN/GaN HEMTs devices are studied intensively for applications such as high power microwave devices used in satellite communication systems and fixed wireless access systems. One of the most important issues with these applications is efficiency and, in recent years with the progress of harmonic-tuned amplifiers such as Class E, F and J amplifiers, high efficiency performance can be achieved with GaN devices. Efficiency of the device is greatly affected by the current-collapse phenomenon and can be generally prevented by employing source field plate in the device. In this paper, we report on the effects of epitaxial wafers and device structures on drain efficiency. The devices were evaluated using a third harmonic tuning active loadpull system.

### **Experiment**

Two kinds of AlGaN/GaN epitaxial wafers were used in this study, named “Epi wafer A” and “Epi wafer B”. The wafers were grown on SI SiC substrates by MOCVD with a difference in the GaN buffer layer. Figure 1 shows the measured photo-luminescence spectrums of the two wafers where yellow luminescence (YL) can be seen in “Epi wafer A”, implying that it has considerably high-density trap states. Three device structures as shown in figure 2 were then fabricated on both wafers, they were (a) without source field plate, (b) with source field plate  $L_{sfp}=0.5\mu\text{m}$  and (c)  $L_{sfp}=1.5\mu\text{m}$ . All devices have the same gate length ( $L_g$ ) of  $0.6\mu\text{m}$  and a total gate width of  $540\mu\text{m}$  ( $270\mu\text{m} \times 2$ ). A curve tracer was used to evaluate the DC current collapse of the devices and a harmonic tuning active loadpull system used to determine their drain efficiency. Figure 3 illustrates the block diagram of the loadpull system which comprises of third harmonic active tuners. The devices biased at 40V drain supply were evaluated at a fundamental frequency ( $f_0$ ) of 3.0GHz.

### **Results and Discussions**

The drain current-voltage characteristics of the HEMT are as shown in figure 4. The gate voltages were applied from +1V to -4V with a step of 1V. The red color curve shows the current characteristics swept to a maximum drain voltage of 10V and the blue curve to 100V. It can be seen that in contrast to “Epi wafer B”, current collapses were prominent in all the devices fabricated on “Epi wafer A” with a slight improvement for devices with source field plate. Figure 5 shows the measured drain efficiency of the devices. For devices fabricated on “Epi wafer A” which has high-density trap states, it can be seen that the drain efficiency increases with longer source field plate. This can be attributed to the reduction in gain at the second- and third-harmonic frequencies ( $2f_0=6\text{GHz}$ ,  $3f_0=9\text{GHz}$ ) when the source field plate length increased. In contrast, device fabricated on “Epi wafer B” which has low-density trap state has higher drain efficiency as the source field plate length reduced. The device without source field plate has an efficiency of 84% which is about 20% higher than that of “Epi wafer A”.

In this study, we have shown that low-density trap epitaxial wafer is crucial to a GaN device performance. It can produce device with minimal current collapse phenomenon which is not required source field plate to improve its efficiency.

