Productivity Improvement Using Plasma-based Die Singulation

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The motivation of lowering device manufacturing costs while maintaining high performance is constant. Included in the objective is the requirement that yield and reliability be optimized. The concurrent trends of GaN on silicon and thinner substrates introduce new challenges.

In general, thinner substrates are placing significant constraints on traditional dicing technology using saws. For substrates with thickness of less than 100µm, productivity is compromised by the serial nature of the process and the reduction in linear saw cutting speed. A compounding issue with saws is the induced cracking and resulting decrease in die strength. A third limitation with saws is the street width required due simply to minimum blade size. Singulation using lasers has been introduced with limited success due to a variety of complex issues including alignment, incompatible materials (absorption/reflection), contamination (ablation), and heat affected zones (HAZ).

In this work we introduce an approach that addresses these issues using plasma based etching on industry standard tape frames. Significant increases in productivity and yield are achieved while greatly lowering manufacturing costs. This translates not only to higher throughput with more wafers per hour but additionally more die per wafer and enhanced yields due to the elimination of saw and laser damage. Although these benefits can be realized on any device type fabricated on thin silicon substrates, this work will focus on GaN on silicon for power and solid state lighting (LEDs).

Presently, the typical widths of streets to accommodate saw technology are between 50µm to 100µm. This new method is only limited by downstream of pick and place but can enable street sizes of less than 5µm. For this practical reason we typically utilize street widths of 10µm to 15µm. This reduction adds significant active area that can be used for additional die per wafer or larger die. The Table shown below for 150mm and 200mm wafers provides an example summary of benefits for plasma dicing. In this example, comparing 70µm streets to 15µm streets and fixing the die size to 3mm x 3mm, the active area gained per wafer is ~ 4% and corresponds to a yield increase of over 100 additional die on a 200mm wafer.

	150mm wafer	200mm wafer		
	Saw (70µm street)	Plasma (15µm street)	Saw (70µm street)	Plasma (15µm street)
Additional die per wafer	-	64	-	115
Throughput (wph)	3.2	5.1	1.8	5.1
Added active area (%)	-	3.7	-	3.7
Saved monthly wafer starts	-	1488	-	2407

Table 1: Example of productivity comparison between plasma and saw dicing. (100µm thick silicon wafer, 3mm x 3mm die, assumed saw speed of 15mm/s)

Saws and lasers continue to encounter challenges as wafer thicknesses decrease. The figure below illustrates the significant gain in die strength achieved with plasma dicing for 120µm thin substrate. An improvement factor of 3x versus laser and an impressive 9x improvement versus saw is observed. This result suggests that further substrate thinning is possible with associated gains in device performance and yield.

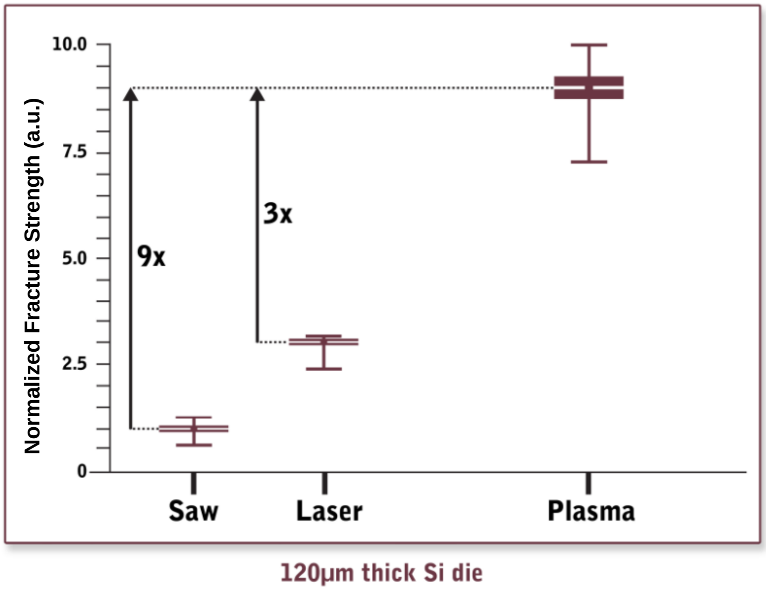

Figure 1: Die strength comparison between plasma, saw, and laser dicing.

A unique aspect of plasma dicing is that it is parallel-based and not constrained to orthogonal x/y coordinated streets. This allows flexibility in specific die design (shape) and die layout on the wafer. Examples of this flexibility, such as shown in Figure 2, will be presented.

Figure 2: (left to right) a) 100mm wafer on dicing tape prior to etching, b) plasma dicing of circular diodes, c) fully plasma singulated devices with through wafer holes.