High Speed Highly Parallel Multi-site GaAs Diesort Testing

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Abstract

On-wafer DC screening of GaAs integrated circuit die is crucial for cost-effective fabrication of multi-chip modules. However, cost of that test must be tightly controlled. Traditional switch matrix – based test systems have small numbers of DC IV source measurement units (SMU's). Users of those systems can reduce test time and lower cost by contacting multiple (typically 4, 6, or 8) die at each step then testing them serially. That reduction is only in the stepping time component of total test time.

We report on our development of high-SMU-count Keithley S500 parallel test systems for this application. Our systems are configured in 6 parallel groups each with 10 SMU's for hex-site diesort testing of our 150 mm GaAs wafers using cantilever, vertical, or pyramid probe cards. Each group's SMU's are arranged with a single master SMU and 9 slaves, giving 10 independent SMU's per site. The test code is pre-loaded into the master SMU of each group and is executed under its control when strobed by the system controller. Each die under test is then tested essentially simultaneously with only status checking and data transfer done serially.

Our first approach used the script language resident in these SMUs to perform measurements with sequential commands at runtime. This combined with quad-site parallel test lead to an estimated 10-fold increase in the throughput of the traditional single site switch matrix-based systems. Further optimization followed, increasing sites contacted to 6 and employing best practices in test code to further speed up the test.

Using the parallel groups of the Keithley S500 with hex-site probing, we have demonstrated 100 msec total test time per die (total time per wafer divided by number of die tested). This has substantially reduced test time and cost for our HBT Power Amplifier wafers, which typically have 15 – 30,000 testable die per wafer.

From a manufacturing cost-of-test perspective, these 6x10 SMU test systems are built from arrays of 30 relatively inexpensive dual-SMU boxes with most of the system definition and control done in commercial off-the-shelf software, so capital costs are comparable to large switch-matrix based testers. By developing a commercially-integrated system, we have preserved a test process traceable to calibration standards and with a viable maintenance strategy. Finally, by achieving higher throughput with multi-site parallel test and the Keithley S500 system architecture, we need fewer test systems for given wafer volumes, gaining significantly higher test productivity and lower test cost per die.