Low-Voltage and Low-Cost ZnO Based Ultra-Thin-Film Transistors

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Introduction

The transfer characteristics of a low-voltage and easily manufacturable novel zinc oxide (ZnO) extremely thin film transistor (TFT) are investigated. The active and insulating films are fabricated on a less than ideal surface using atomic layer deposition (ALD) without exceeding 130 ºC, making this process compatible with a wide variety of applications. They are considered "ultra" thin because their maximum vertical height does not exceed 100 nm from the top-gate to the source/drain-bottom. Furthermore, the ZnO film exhibits a relatively high doping concentration (>10^{17} cm^{-3}) which allows for the scaling of the drain-gate spacing with a manageable series resistance [1]. In this study, we examine the electrical behaviour of two different top-gate overlaps: the essential switching metrics, threshold voltage V_{TH}, current on/off ratio ($I_{ON/OFF}$), subthreshold slope (SS), and drain induced barrier lowering (DIBL) are presented and contrasted. The goal of this work is to illuminate the self-aligned architectural affects on electrical performance. Ultimately, these types of devices enables effortless integration in, for example, the emerging field of low-voltage OLEDs for display technology, printed and flexible electronics and low-power energy harvesting integrated circuits [2].

Purpose

This work examines the large-signal effects of sizeable overlaps of the gate over the source region of a top-gated staggered high-κ-oxide/ZnO TFT. The extremely small thickness (<100 nm) allows for easy integration into numerous emerging applications, although there are challenges in controlling its behaviour. We aim to improve the electrical performance of these ultra-thin devices architecturally. The full realization of this architecture will ensure minimal dependence on the device characteristics with respect to material properties.

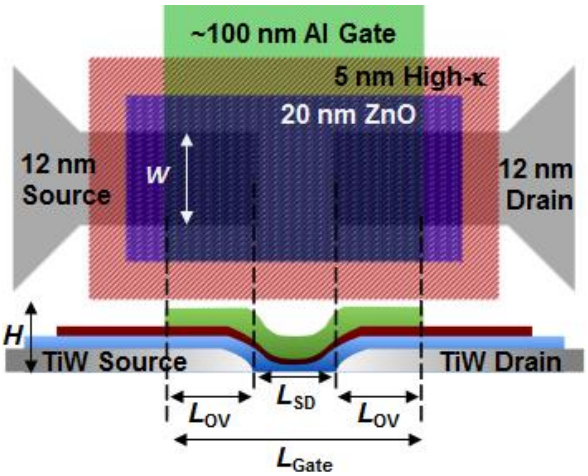

Fig. 1: Top-down and cross-section view of the top-gate ZnO TFT device; common dimensions include L_{SD} = 10 µm, W = 10 µm, H = 100 nm. The critical parameter in this study being L_{OV}.

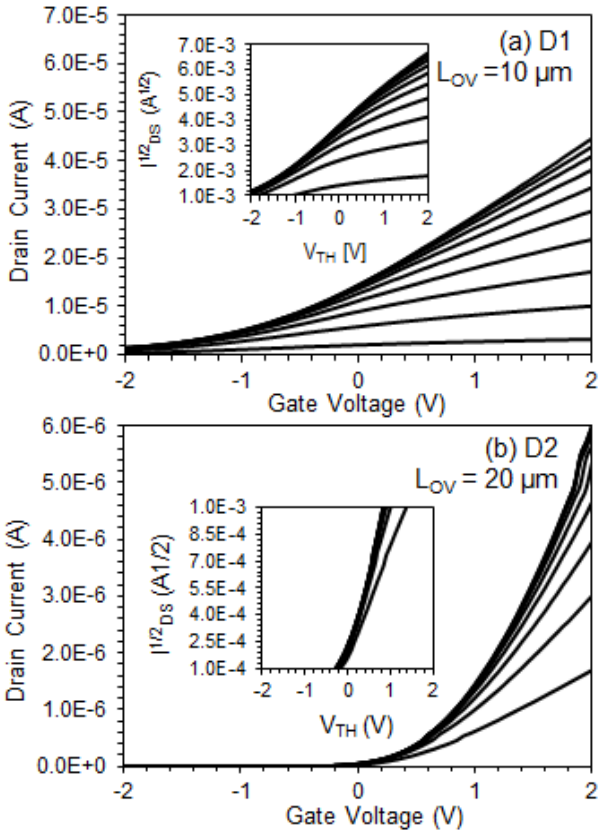

Fig. 2: Transfer characteristics of device (a) D1 with L_{OV} = 10 µm; and, (b) D2 with L_{OV} = 20 µm. The inset shows the device's $\sqrt{I_{DS}}$ intersection with its V_{TH} at various V_{DS}.

What we present and elaborate on are:

i. Better transfer characteristics for larger overlaps
ii. Major improvement in $I_{ON/OFF}$, SS and DIBL
iii. Enhancement properties with ZrO_2 as gate insulator

Methods and Manufacturing

The manufacturing goal for these ultra-thin devices was to simplify the process for extremely low costs while still maintaining respectable device characteristics. The critical paramerter here is the gate-to-source overlap. However, the gate-to-drain distance can also be scaled to manipulate breakdown behaviour of the device.

We first deposited 12 nm of titanium tungsten (TiW) metal for the source and drain on amorphous silicon dioxide/silicon wafer. The active layer ZnO is a thermal ALD film grown at 130 ºC, as is the high-κ dielectric gate oxide deposited *in-situ* with thicknesses of 20 nm and 5 nm, respectively. An aluminum top-gate TFT was constructed, with a gate-to-source and drain overlap of L_{OV} 10 µm, with L_{Gate} of 22 µm (designated D1) and 20 µm with L_{Gate} of 42 µm (D2). Common dimensions are W = 10 µm, and L_{SD} = 2 µm, with a maximum device height of H = 100 nm. The top-down and cross-sectional view with relevant dimensions of the final device are shown in Fig. 1.

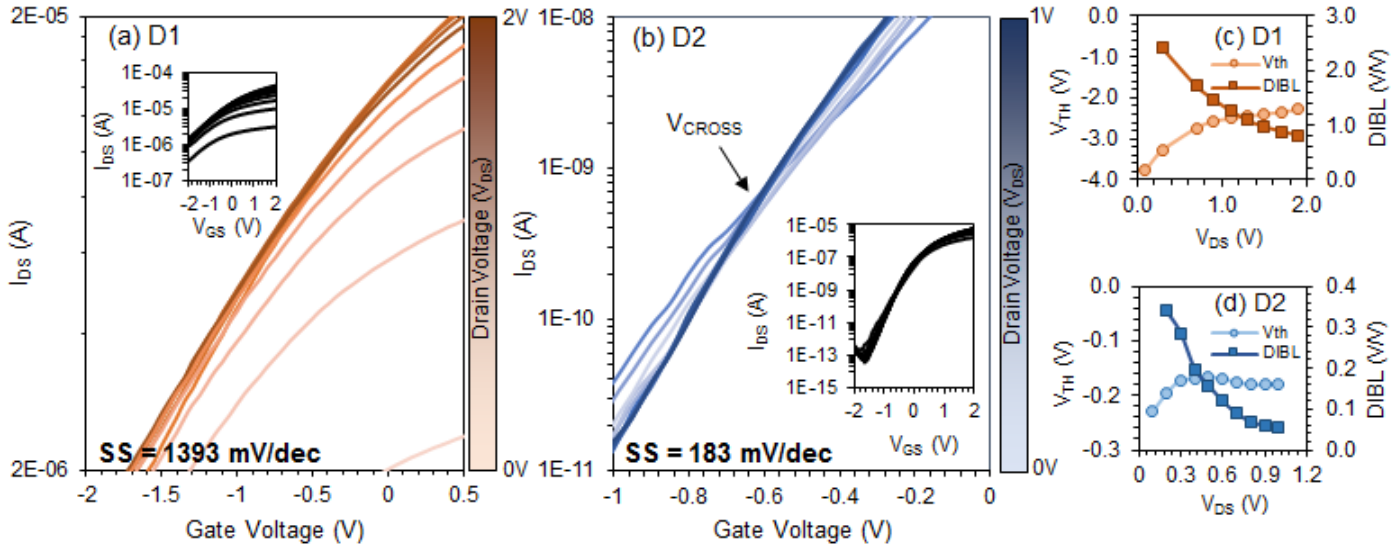

Fig. 1: Subthreshold swing SS and DIBL observed in the transfer characteristics for (a) D1 with L_{OV} = 10 µm and (b) D2 with L_{OV} = 20 µm and V_{CROSS} indicating the voltage where the DIBL reverses, the insets shows the full transfer curve in a linear-log scale; (c) the variance of threshold voltage V_{TH} and DIBL on drain voltage V_{DS} for D1 and (d) D2.

Results

Fig. 2(a) and (b) shows the transfer characteristics (IV_{GS}) of gate overlaps 10 µm and 20 µm, with varying drain-to-source voltage V_{DS}. The inset within each figure shows the $\sqrt{I_{DS}}$ dependence on the gate voltage, which determines the threshold voltage V_{TH} of each device through a linear fit which intercepts at the V_{TH} of the device. D1's behaviour is characteristic of a depletion-mode transistor, with a negative threshold voltage of -2.3 V; and, while D2's threshold voltage also exhibits a small negative threshold of -0.2 V, this can be rectified by either increasing the oxide's thickness or improving the quality of the oxide-semiconductor interface.

The $I_{ON/OFF}$ and SS are also much improved with an increased overlap: D1 was evaluated at $I_{ON/OFF\text{-}D1} = 10^2$ and SS_{D1} = 1392 mV/dec, while D2 revealed that $I_{ON/OFF\text{-}D2} = 10^7$ and SS_{D2} = 183 mV/dec as shown in Fig. 3(a) and (b), respectively.

Additionally, the drain-induced barrier lowering (DIBL) was also closely examined for both devices. The comparison between D1 and D2 are shown in Fig. 3(c) and (d). It is apparent that D2's larger overlap provides a significant improvement. Whereas the DIBL evaluated for D1 was a 1.4 V/V, D2 exhibited a $DIBL_{D2}$ of 0.06 V/V.

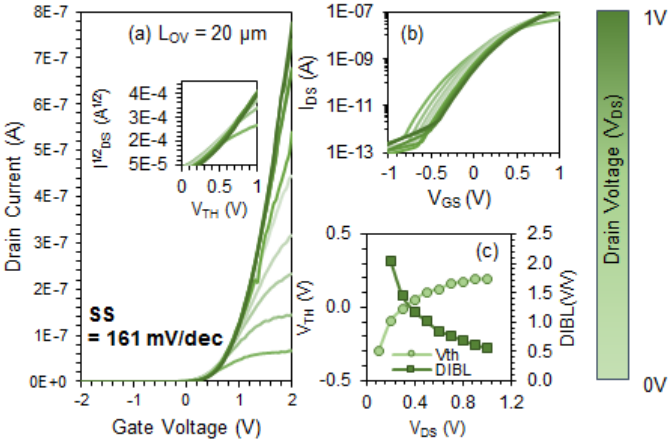

Fig. 2: Top-gate TFT with ZrO_2 (a) Transfer characteristics, the inset indicates the V_{TH} for the device; (b) log-transfer curve which shows the positive crossing point V_{CROSS}; and, (c) threshold voltage and DIBL versus drain voltage V_{DS} (V).

It is interesting to note that, unlike the transfer curve of D1, in D2, before a certain gate voltage, we can observe that the output current I_{DS} is lower for higher V_{DS}, until it reaches a "crossing point" where after it behaves as one would expect given the DIBL effect. For D2, the V_{GS} where the crossing point V_{CROSS} is observed is ~-0.6V (Fig. 3(b), captioned marker).

From closer inspection of Fig. 3(b), we posit that, if we are able to realize an enhancement mode TFT by shifting the V_{CROSS} more positively, it is possible to take advantage of the "reverse" DIBL phenomenon, where increasing V_{DS} also increases the V_{TH}. Although DIBL does not affect SS, by manipulating V_{CROSS}, it can indirectly improve the subthreshold slope.

Because no such effect has been reported with a thicker dielectric, with the thinnest known at 25 nm in [3], we deposited instead a zirconium oxide (ZrO_2) insulator, which is electronically similar to HfO_2, with the same thickness of 5 nm.

Our results presented in Fig. 4 show a much improved transfer characteristics including a positive V_{CROSS} = 0.7 V, V_{TH} = 0.2 V, $I_{ON/OFF} = 10^6$, SS = 161 mV/dec and DIBL = 0.5 V/V. Thus, we show that to better control the transfer characteristics of the low-voltage, low-cost and extremely thin device, extending overlaps and utilizing thin high-κ gate dielectrics on a ZnO-based ultra TFT can improve its switching performance substantially while maintaining a higher channel doping concentration.

References

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