

Fabrication of GaN MISHEMTs Fabricated From GaN Grown By MOCVD on High Resistance 200mm <111> Si Substrates

Jeffrey LaRoche¹, Kelly Ip¹, Mark Breen², Yu Cao³, John P. Bettencourt¹, Doug Guenther², Gabe Gebara², Oleg Laboutin³, Chien-Fong³, Tina Trimble², Wayne Johnson³ and Thomas Kazior¹

1. Raytheon IDS Microelectronics, 362 Lowell St., Andover, MA 01810
Email: jeffrey_r_laroche@raytheon.com Phone: (978)-684-8636
2. Novati Technologies, Inc., 2706 Montopolis Drive, Austin, TX 78741
3. IQE, 200 John Hancock Rd, Taunton, MA 02780

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ABSTRACT

Raytheon has demonstrated 0.25 μ m GaN MISHEMTs fabricated on 200mm high resistance <111> Si substrates. The GaN epitaxial layers were grown by metal organic chemical vapor deposition (MOCVD), by IQE, the leading commercial GaN epi vendor and, display low wafer bow ($\leq 23\mu$ m) and excellent mobility (1,600 cm²/V*s). These wafers were fabricated in a commercial CMOS foundry (Novati Technologies) using a fully subtractive, Au-free, Si-like fabrication approach.

Over the last decade gallium nitride (GaN) has garnered considerable interest for use in power electronics and high power density RF applications. The use of large feature ($\geq 1\mu$ m gate, $\geq 10\mu$ m source/drain gap) horizontal GaN HEMT transistors in switching applications is projected to be attractive for drain voltages up to ~600V.

In the RF application space, MMICs fabricated from deep submicron GaN HEMTs ($\leq 0.25\mu$ m gate, $\leq 3\mu$ m source/drain gap) have demonstrated power amplifiers (PAs) and low noise amplifiers (LNAs) with excellent characteristics at frequencies ranging from S-band to W-band and beyond. In general the GaN PAs exhibit gain and efficiencies equivalent to GaAs PAs at ~5X the power density. Meanwhile GaN based LNAs demonstrate excellent noise figures, but with much higher linearity and survivability than their GaAs based counterparts. Finally, it should be noted that the device cross sections developed for RF applications could be adapted to low voltage, high frequency power switching applications and enable the use of smaller transformers.

As GaN device technology matures and proliferates into commercial and defense markets, cost reduction efforts will become increasingly more important. To that end, manufacturing GaN devices in a Si foundry with high yield subtractive processes, large diameter wafers, and a (Moore's law based) culture of rapid development seems like a natural evolutionary path for the technology. This is particularly

true for medium power applications suitable for fabrication on 200mm Si substrates where the enhanced thermal conductivity of not yet available 200mm semi-insulating SiC substrates is not needed.

Building on our previous GaN on Si work^{1,2,3,4}, Raytheon designed a deep submicron, Au-free subtractively processed device cross section and released the mask at Novati, its partner Si foundry, in 2013. This coplanar waveguide (CPW) 0.25 μ m process cross section utilized an ALD high k gate dielectric to reduce gate leakage, MIM capacitors, thin film resistors, and a three metal Cu interconnects (Back-End-Of-Line (BEOL)).

In order to minimize gate leakage without negatively impacting critical RF device characteristics a charge balance model was used to design Schottky layer thickness in conjunction with the gate dielectric stack. This was done so that the overall gate capacitance, I_{DSS} , I_{MAX} , and V_T were similar to typical microwave GaN HEMT processes.

The material was grown by the commercial epi vendor, IQE. The material had excellent mobility (1,600 cm²/V*s) and critically for device fabrication tools in a 200 mm Si foundry, very low wafer bow ($\leq 23\mu$ m) as shown in figure 1.

The processing for this demonstration was done entirely in Novati's 200 & 300mm Si foundry, in a completely subtractive manner using Au-free processes. More importantly, this was done at Novati's foundry without contaminating or otherwise adversely affecting a diverse array of background Si based products. A photograph of a 200mm GaN on Si wafer in process inside the Si foundry is shown in figure 2. Transistor functionality is shown at post gate in figure 3.

To our knowledge, this is the first report of a 0.25 μ m gate GaN on Si MISHEMTs fabricated with a fully subtractive, Au-free process in a 200mm Si foundry with Cu interconnects (BEOL).

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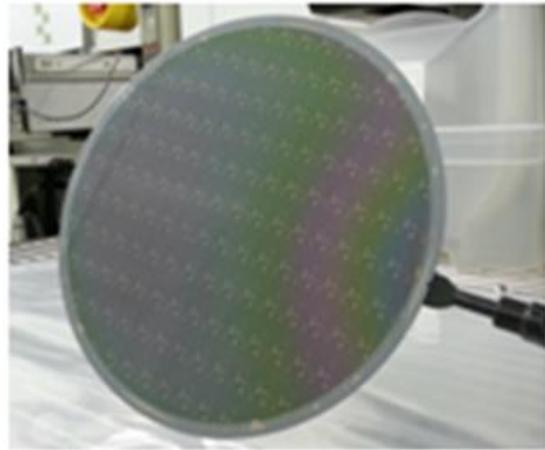


Figure 2. Processed 200mm GaN on Si wafer in Novati's Si Foundry.

IQE Run No.	200mm Si Wafer Bow after GaN Epi (μm)
38-gos-164	-19.6
38-gos-211	-2.6
38-gos-216	2.4
38-gos-218	17.6
38-gos-221	-22.5
38-gos-221	-19.5
38-gos-221	-20.9
38-gos-225	7.8
38-gos-225	20.5
38-gos-225	19.0

Figure 1. <111> Si wafer bow after GaN on Si epitaxial growth. These wafer bow characteristics are well below the wafer bow limitations of 193nm lithography tools.

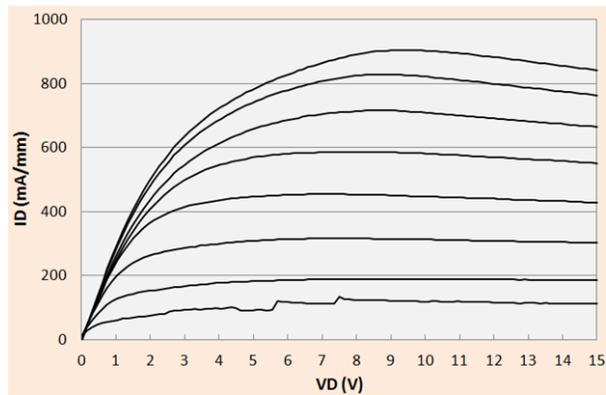


Figure 3. Transistor I-V characteristics for a fully functional, Au-free, GaN MISHEMT on 200 mm Si substrates fabricated in Novati's Si foundry.