Need for Defects in Floating-Buffer AlGaN/GaN HEMTs

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Purpose of Work

Carbon (C) is a deep-level p-type acceptor in GaN and has been used successfully in high-voltage AlGaN/GaN HEMT processes to generate a semi-insulating buffer for off-state leakage and breakdown suppression. However, p-type doping has also been linked to dynamic R_{ON} dispersion and current-collapse (CC) due to the absence of an Ohmic contact to the floating buffer region [1]. We demonstrate that CC- free C-doped HEMTs can be realized using epitaxial defects which short the floating buffer to the 2DEG.

Approach

AlGaN/GaN HEMT devices from two similar processes were compared, but with identical C-doped GaN on Si epitaxy. Wafer A showed strong CC, whereas Wafer B was essentially CC free (Fig. 1), while they were identical under DC operation. Novel ramped and pulsed substrate bias measurements were used to exclude surface effects, monitor the dominant buffer related CC and vertical leakage, and identify the leakage path location. Simulation of CC with the inferred localized leakage paths under the source/drain contacts showed excellent agreement with experiment.

Results and Discussion

Pulsed V_{SUB} induced channel current transient [2] and conventional CC measurements showed the same time-constants and wafer dependence indicating a common dispersion origin and clearly demonstrating that the responsible defects were located in the buffer (Fig. 2). Hysteretic behavior in novel ramped V_{SUB} measurements (Fig. 3) indicated that the potential in the buffer was pinned by leakage through the reverse biased P-N (buffer to 2DEG) junction once the vertical applied electric field exceeded a critical value. Varying the source-drain gap proved that for Wafer B the leakage occurred over the entire surface, whereas for Wafer A there was strong leakage only under the contacts [3]. The resulting partially floating buffer in the center of the device, is the underlying reason for wafer A and not wafer B showing significant CC.

GaN on Si is highly defective with $>10^{9}cm^{-2}$ dislocations, which can act as trap assisted tunneling paths, as seen in LEDs [4]. The different leakage paths between wafers A and B likely arose from differences in the fabrication process electrically activating/deactivating mixed and screw dislocations (Fig. 4).

The effect of a leakage path between the contacts and the semi-insulating buffer was simulated. The GaN resistivity and C acceptor level 0.9eV above the valence band were determined experimentally by dynamic transconductance [5], and were used in the simulation. A floating p-type buffer resulted in an extreme CC (Fig. 5a), whereas adding a short only under the contacts representing the measured active defect location, reproduced the behavior of Wafer A (Fig. 5b). A uniform distribution of leakage paths as in Wafer B suppressed the build-up of any buffer potential, and resulted in excellent performance (Fig. 1b).

Conclusions

C-doped buffers can deliver low current collapse, however fabrication processes must ensure that they do not suppress defect-induced leakage. Contrary to normal expectations, vertically conducting defects are essential for the functioning of lateral GaN-on-Si power devices.

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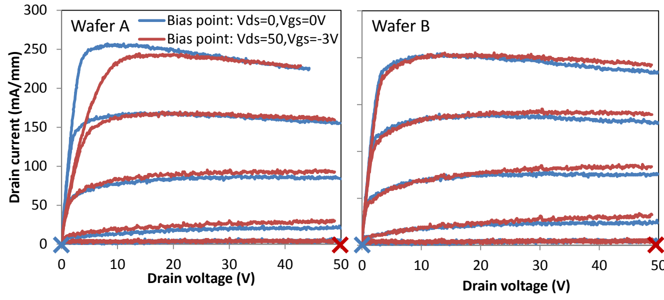

Fig. 1: Double pulse (DIVA) measurement of AlGaN/GaN HEMTs from ON (blue lines V_{DS}=0,V_{GS}=0V) and OFF (red lines V_{DS}=50,V_{GS}=-3V) quiescent bias points. Pulse durations 1µs/1ms, V_{GS}=0,-0.5 … -2.0V. Wafer A shows current-collapse, whereas Wafer B is almost ideal.

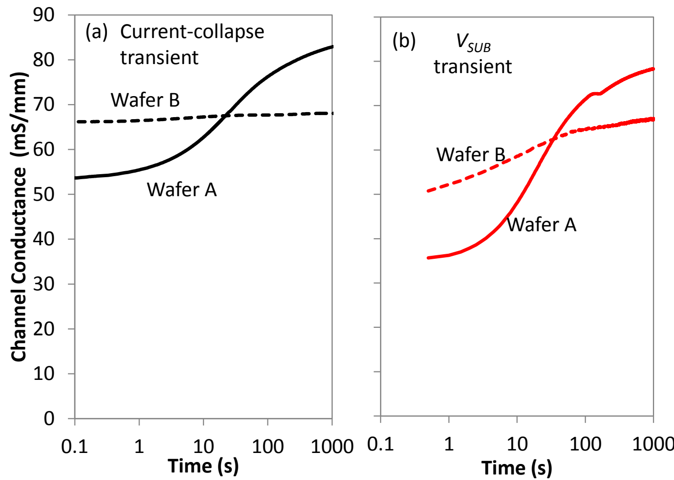

Fig. 2: Drain current transients (a) following step from OFF state (V_{DS}=50V, V_{GS}=-3V) to ON state (V_{DS}=1V, V_{GS}=0V), (b) following step from V_{SUB}=0 to -200V with V_{DS}=1V. Similar time-constant and wafer dependence is observed indicating a common transient origin.

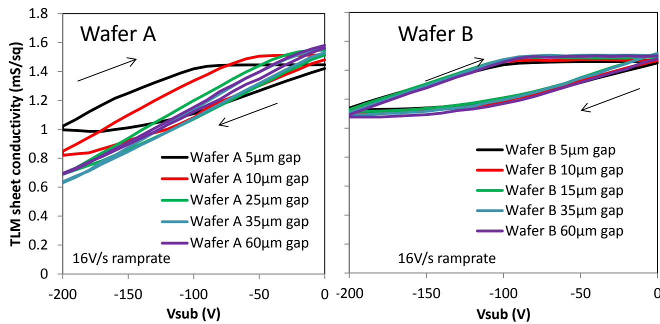

Fig. 3: Sheet conductivity of ungated structures of varying width as V_{SUB} is swept from 0 to −200V and back to 0V. The current is sensitive to the field below the 2DEG, so a saturation in current indicates that the buffer potential has stopped changing capacitively with changing V_{SUB}. Once saturated, the vertical leakage current equals the displacement current.

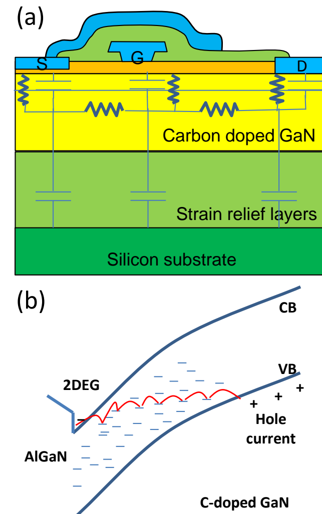

Fig. 4: (a) Schematic showing the vertical and lateral leakage and capacitive paths important in these GaN HEMTs. (b) Trap assisted tunneling process along a dislocation to inject holes from the 2DEG into the buffer during swept V_{SUB} measurement.

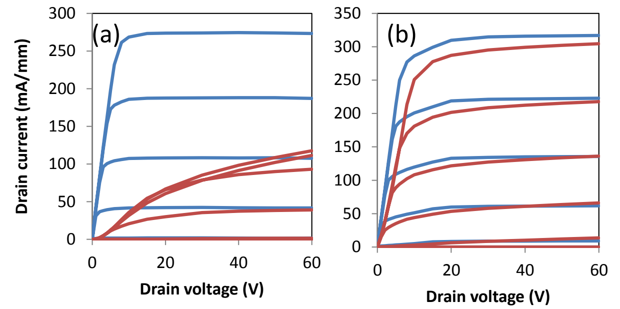

Fig. 5: Simulated double pulse (DIVA) measurements for the same conditions as in Fig. 1. (a) floating p−type buffer, whereas (b) has a P++ shorting region to the buffer under the source and drain. Allowing the buffer to float results in extreme CC, whereas shorting the buffer at the source/drain allows charge to accumulate in the buffer only at the center of the device resulting in the moderate, but still unacceptable, CC seen in (b). The results in (b) reproduce those measured in Fig. 1a.