The First 0.2μm 6-Inch GaN-on-SiC MMIC Process

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There is an increasing demand for high power GaN-on-SiC technology for both military and commercial microwave applications. The need to reduce chip costs of GaN MMICs has become a driving force as their use for power applications becomes the norm. One method is to increase the wafer size from the standard 4" (100mm) diameter to 6" (150mm) to provide substantially more area for a lower unit chip cost (see Table I). The conversion to 6" is further justified with the 6" GaN epi cost approaching the 4" cost due to volume demand. In addition to reducing cost, the 6" line has several advantages - better visual and line yield due to increased automation and reduced number of wafers required for qualification. BAE Systems has been working on a 6" GaAs PHEMT technology since 2003. Based on the extensive 6" GaAs experience, we have developed a 0.2μm GaN MMIC process on 6" SiC substrates, as shown in Figure 1.

The 0.2μm 6" dual field-plate (DFP) GaN-on-SiC MMIC fabrication mostly utilizes automated cassette-to-cassette equipment in the foundry, reducing manual wafer handling for higher yield. BAE Systems GaN epi is based on an AlGaN/GaN structure with a thin GaN cap layer and Fe-doped GaN buffer. The material structure is designed to provide a high sheet charge density for high full channel current and output power, while maintaining good reliability. The MOCVD 6" GaN epi has low density of defects - most are substrate related micropipes and polytypes. The sheet resistance uniformity of the 6" wafers is ~1.2% - slightly better than the 4". Al% uniformity of better than 1% from the 6" AlGaN/GaN HEMT structure has also been achieved. The 6" GaN wafer is 500μm thick – similar to the 4" wafer. Epitaxial wafer warping was initially a challenge for the 6" wafers due to the reduced thickness to diameter ratio compared to 4". A set of DOEs was carried out and IQE has successfully reduced the epitaxial wafers' bow and warp from >100μm to ~40μm over the 6" wafers, suitable for wafer processing (see Figure 2.)

The 6" GaN wafer has a notch which is 45° off from that of the industry standard 6" GaAs PHEMT wafer. Some of our 6" GaAs tools failed to recognize the GaN notch due to wafer transparency and the different notch position. We also observed a substrate "leakage" (i.e., leaking photoresist through micropipes in the SiC substrates during lithography process) on some early wafers. After resolving these issues, the remaining effort was largely put into optimizing the existing 4" GaN mesa, ohmic, nitride deposition and via hole formation processes using 6" tools to achieve good uniformity and yield over 6" wafers.

Figure 3 is a SEM photograph of the fabricated 0.2μm DFP GaN devices. The 0.2μm gates and field plates are formed through electron beam lithography. Shown in Figure 4, the GaN HEMT exhibits averaged maximum current of 1,124 mA/mm, extrinsic transconductance of 372 mS/mm at a drain bias of 10V and pinchoff voltage of -3.1V. Two-terminal gate-to-drain breakdown of >90V was measured, similar to the 4" one. These DC characteristics are all within ±5% of the 4" GaN ones. Table II shows the tight distribution and near 100% spec yield of device DC characteristics. The tight distribution and high process yield are attributed to the excellent material quality and improved manufacturability obtained by utilizing the 6" foundry line.

In this paper, we will present a detailed comparison of the performance matrix obtained from 4" and 6" substrates. The parameters include control charts of sheet resistance (R_{sh}) and uniformity and AlGaN

barrier mole fraction and thickness uniformity. Atomic force microscopy (AFM) images and nSPEC microscopic maps for larger surface defects will also be compared. We will discuss the 6" GaN MMIC fabrication process and report device characteristics and yield. These results will be compared to the existing 4" baseline.

Table I. Anticipated cost advantage of 6" vs. 4" processes (normalized to 4")

	4-Inch	6-Inch
Usable Wafer Area*	1	2.4
Process Cost	1	1.2
Epi Cost	1	1.2
Chip Out Per Lot	1	2.4
Chip Unit cost**	1	0.5

* Excluding 5mm around edge circumference of wafers due to epi/processing ring. ** Assuming processing cost = ¾ total cost and epi cost = ¼ total cost.

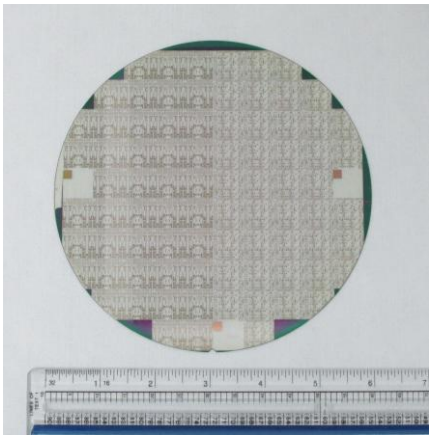

Fig. 1 A fabricated 6" GaN HEMT MMIC wafer.

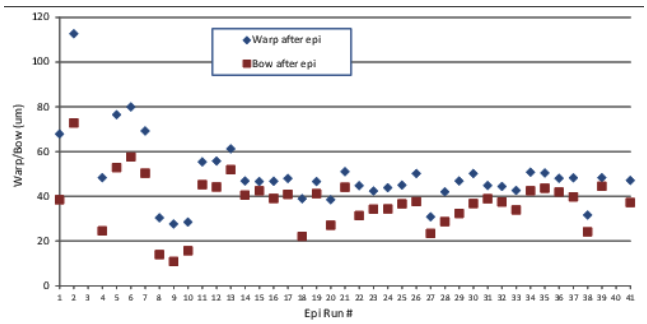

Fig. 2 Improved warp/bow (~40µm) from 6" GaN epi wafers.

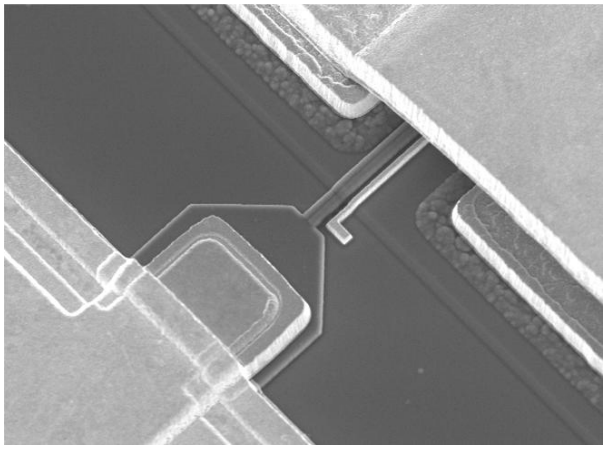

Fig. 3 0.2µm dual field plate GaN device.

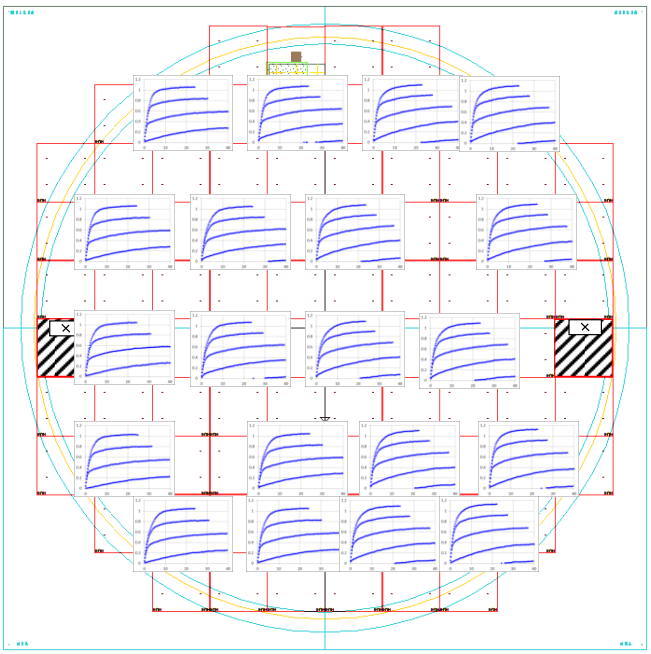

Fig. 4 Mapping of 0.2µm GaN HEMT pulsed I-V

Table II. 0.2µm GaN HEMT device uniformity and yield.

Parameter	4-Inch Value	6-Inch Value	6-Inch Spec Yield
I_{max} (mA/mm)	1075 (±10%)	1124 (±5%)	100%
g_m (mS/mm)	355 (±10%)	372 (±5%)	100%
V_{po} (V)	-3.3 (±5%)	-3.1 (±5%)	100%
V_{bd} (V)	>90	>90	80%

I_{max}: full channel current, g_m: peak transconductance, V_{po}: pinchoff voltage, V_{bd}: breakdown voltage at I_d 1mA/mm. Spec yield: 30 sites from 6-inch wafer.