High Breakdown Voltage ZnO Thin Film Transistors Grown by Low Temperature Atomic Layer Deposition

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Abstract

Low temperature atomic layer deposition processes (< 130°C) are employed for the fabrication of ZnO source-gated thin film transistors (SGTFTs) that utilize a TiW Schottky barrier source contact and a thin (~ 5nm thick) high-κ gate dielectric. The devices demonstrate good transistor characteristics with mobilities as high as 5 $cm^2V^{-1}s^{-1}$. High breakdown voltages exceeding 30 V for a gate-to-drain spacing of 9 µm were also observed by utilizing this unique device architecture.

INTRODUCTION

Zinc oxide (ZnO) thin film transistors (TFTs) are a promising technology for various electronic applications such as liquid crystal displays (LCDs) [1] and high frequency microwave devices [2] because of their good electrical characteristics. In particular, ZnO-based TFTs have demonstrated moderately high mobilities exceeding that of conventional hydrogenated amorphous silicon (a-Si) TFTs. Moreover, their compatibility with low temperature processes and high transparency in visible light are highly attractive for next generation flat panel display (FPD) technologies such as transparent and flexible electronics.

In this work, a novel device architecture based on the source-gated thin film transistor (SGTFT) architecture [3] is utilized with low temperature atomic layer deposition (ALD) films to fabricate top-gated ZnO TFTs that demonstrate many unique and attractive properties. The ZnO SGTFT device reported herein employed a TiW Schottky barrier for the source contact, which leads to different device operating physics and unique device characteristics compared to the conventional TFT. A key feature of this device was the high breakdown voltages observed for the device dimensions. Based on our measurements, the ZnO SGTFT is a promising route for the manufacturing of high performance TFTs suitable for many applications beyond display technologies.

DEVICE FABRICATION

The top-gated ZnO SGTFTs were fabricated on an insulated silicon substrate. Firstly, 12 nm of TiW was deposited by sputtering and patterned with lift-off to form the Schottky source contact. Thermal ALD was then used to grow the ZnO channel at 130°C with a thickness of 20 nm before it was etched with ferric chloride ($FeCl_3$) for mesa isolation. A 5 nm thick high-κ zirconium oxide (ZrO_2) thin film was utilized for the gate insulator layer, which was deposited by plasma enhanced ALD at 100°C and then patterned with lift-off. Finally, a metal stack consisting of Al/Au (20 nm/60 nm) was sputtered at room temperature and patterned with lift-off to form the ohmic contacts for the gate and drain. No post-deposition annealing was done so as to keep the processing temperature low enough to be compatible with inexpensive flexible substrates. A schematic cross-section image of the SGTFT is shown in Fig. 1. For this study, the device's width (W), source-to-drain distance (L_{SD}), and gate-to-source overlap (L_{SG}) were held constant while the gate-to-drain distance (L_{GD}) was changed to examine its effect on the transistor characteristics.

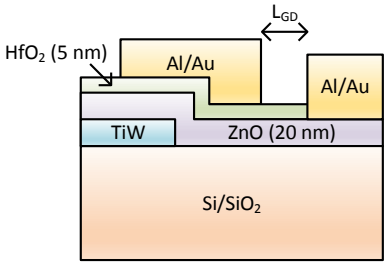

Fig. 1. Cross-section schematic image of the ZnO SGTFT.

MEASUREMENTS AND RESULTS

Fig. 2 shows the output characteristics of the ZnO SGTFTs. The W, L_{SG}, and L_{SD} of the measured devices were 50 µm, 15 µm, and 32 µm respectively; whereas, L_{GD} was varied from 9 µm to 30 µm. All of the devices show good transistor behavior with a clear transition from the linear to saturation regime. The drain current (I_{DS}) during saturation reached ~10^{-5} A. As L_{GD} was varied, we did not observe a noticeable effect on the transistor's output current, which implies the variations in the output characteristics between devices were caused mostly by processing inconsistencies. For instance, it is evident that the device with L_{GD} = 9 µm displayed the highest output impedance of

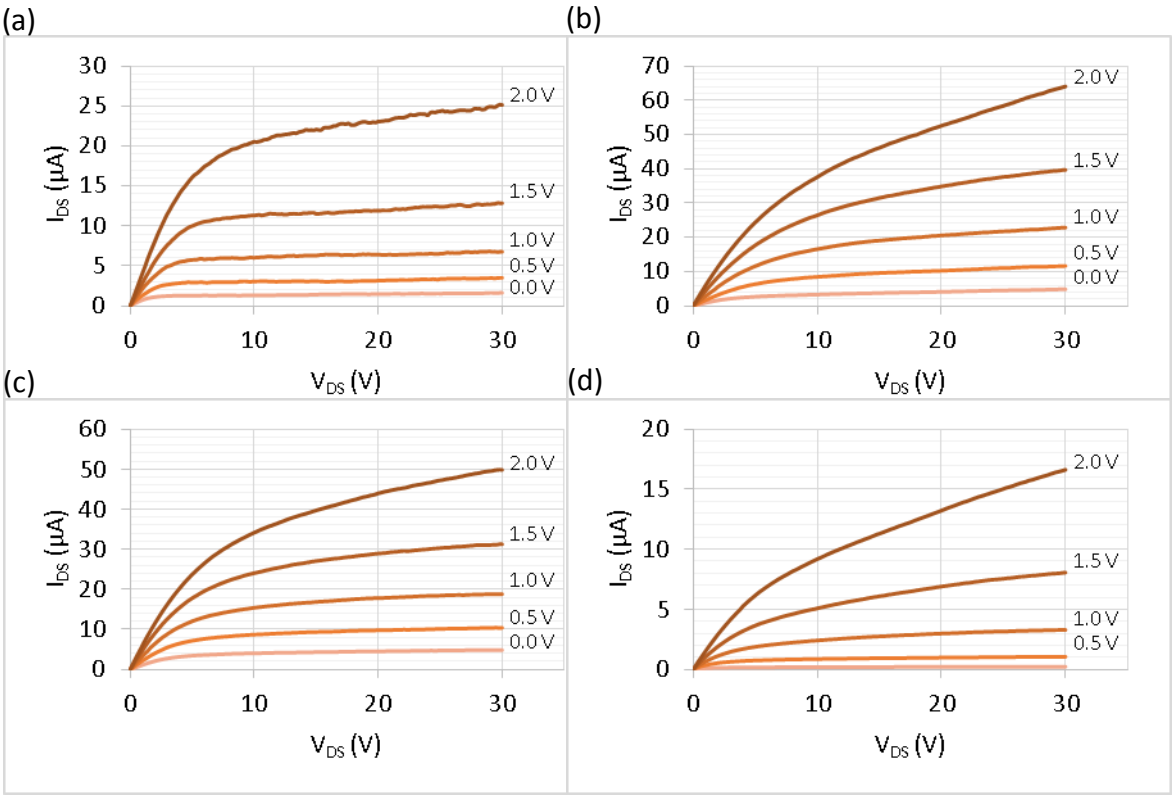

Fig. 2. Output characteristics of the ZnO SGTFTs for a gate-to-drain spacing of (a) 9 μm, (b) 16 μm, (c) 23 μm, and (d) 30 μm.

all the devices (which is seen by the flatness of the curves in the saturation regime). Particularly, the output characteristics of this device most closely resemble the curves expected of SGTFTs [3]. In the SGTFT, when the drain voltage (V_{DS}) is increased, the depletion region from the Schottky barrier formed at the source extends towards the insulator and reduces the concentration of carriers there. Hence, the current can saturate at a lower V_{DS} from being pinched off at the source rather than in the channel. This results in very distinct output characteristics featuring low saturation voltages and high output impedances similar to the curves shown in Fig. 2(a) [4]. Nevertheless, most of the devices depicted in Fig. 2 do not show pure SGTFT characteristics, which implies that the quality of the TiW Schottky barrier at the source was inconsistent and the channel conductance still played a major role in the transistor characteristics of our SGTFTs.

From the square root of I_{DS} vs V_{GS} characteristics at V_{DS} = 30 V, the threshold voltage (V_{th}) and saturation mobility (μ_{sat}) of each device was calculated, and the results are shown in Table I. Moreover, each device's breakdown voltage (V_{BD}) was determined at zero gate bias, and those results are also tabulated in Table I. The devices exhibit high V_{BD} for their device structure, and thus, are highly promising for a variety of circuit applications.

TABLE I.
Summary of the ZnO SGTFT properties

L_{GD} (μm)	V_{th} (V)	μ_{sat} ($cm^2V^{-1}s^{-1}$)	V_{BD} (V)
9	-0.61	3.6	31.8
16	-0.76	4.0	34.6
23	-1.14	3.8	40.5
30	-0.07	5.0	45.7

CONCLUSIONS

We report ZnO SGTFTs featuring a bottom TiW Schottky barrier source contact and a thin ZrO_2 gate dielectric that demonstrate good transistor characteristics with mobilities as high as 5 $cm^2V^{-1}s^{-1}$ and uniquely high breakdown voltages (> 31.8 V) for their dimensions.

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