Wavetek's GaAs Manufacturing in UMC's 6-inch CMOS Fab

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ABSTRACT

Wavetek entered the GaAs foundry service in 2010. The GaAs and CMOS production line are located within UMC's 6-inch CMOS fab and share the same clean room facility. The first phase of conversion will have a total capacity of 36,000 wafers per year. To set up the GaAs line the cross-contamination concern on running CMOS and GaAs (HBT and pHEMT) is addressed in two major areas besides the process tool modification and environmental waste handling : dedicated tool sets and fab personnel, as well as separated MES.
In the end, the HBT and pHEMT process offering for various product applications will be presented also.

INTRODUCTION

UMC is a trusted pure-play CMOS silicon foundry having a broad portfolio of customers and standard foundry offerings. With the increasing demand for mobile data rate and multimedia service in recent years [1], and the fact of CMOS technology migration from 6 to 8-inch for die cost reduction, Wavetek was then founded as a 100% UMC owned subsidiary in 2010 as a pure-play GaAs foundry utilizing the existing UMC 6-inch CMOS factory (Fab6A). The conversion from CMOS line to GaAs is a logical move because 6-inch GaAs MMIC is still the mainstream technology in today's mobile cellular and wireless infrastructure applications[2]. The clean room facility and equipment of Fab6A can also be used for GaAs process with moderate tool conversion. The construction time for the GaAs pilot line and tool conversion took approximately six months, saving roughly one year compared to a brand new fab construction. The technology used to bring up and qualify the process was a cellular HBT process, licensed from GCS in USA [3].

The cross contamination concern of Au and other sensitive materials used in the GaAs process in the CMOS technology is addressed with special care. The containment scheme was a proven solution from UMC manufacturing experience, where in some fabs the aluminum and copper interconnect backend processes co-exist. It requires tremendous manufacturing discipline and methodology. The time it took us to reach technology qualification from the HBT process setup was within one year.

Here, we would like to introduce the key areas that are critical for CMOS to GaAs conversion, and briefly touch upon our technology offering.

- **Environmental Waste Handling**

The GaAs wafer thinning process and wafer sawing process produces a considerable amount of waste water and GaAs powder. A separate waste water treatment system is built to extract GaAs from the waste stream before it merges into the UMC CMOS waste treatment main system. As for the GaAs particles from the dicing process, industrial centrifuges are employed to collect bulk GaAs particles. Figure 1 illustrates the flow of waste water processing.

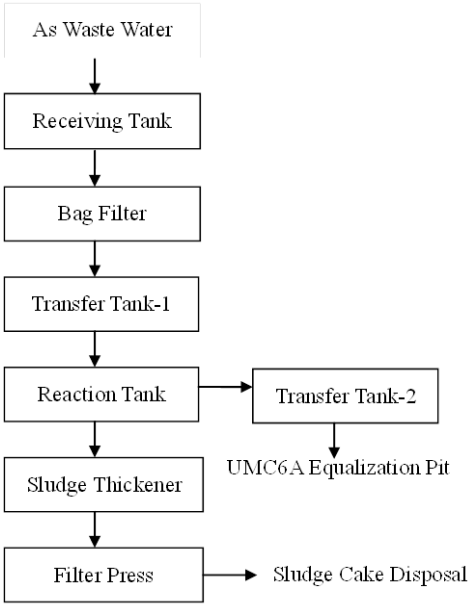


Figure 1 The flow chart of waste water processing.

Wavetek and UMC teams work together with local environmental agencies to reassess the impact of additional

waste from GaAs manufacturing in the end. The mandatory permission application is also an essential procedure of the CMOS to GaAs conversion effort.

- **Dedicated Production Tools/Engineers/Operators**

All tools and equipment used for the GaAs process are dedicated through either new purchasing or retrofitting from the silicon process. More GaAs specific tools, such as wet benches, evaporators, grinding, and laser dicing tools, are new purchases. Other tools, such as photo steppers, SiN deposition , and asher, etc. are retrofitted to 6-inch GaAs notches from silicon line. All GaAs process related tools and equipment are isolated from silicon production with significant color and label differences. Figures 2(a) and (b) show the appearance of wafer box and vacuum pen for GaAs and silicon process line.

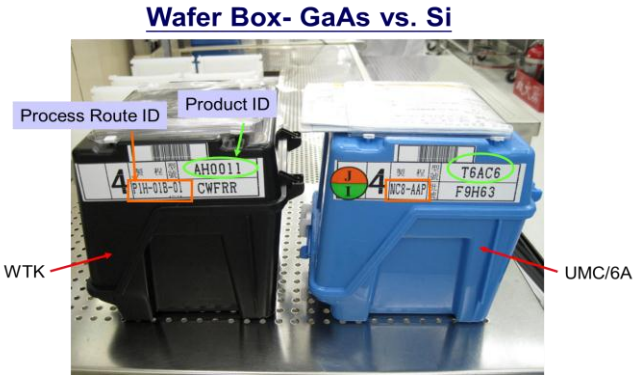


Figure 2(a)

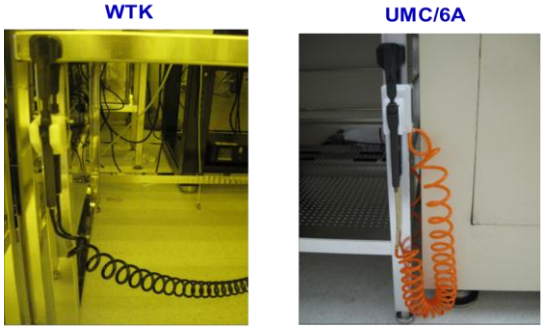


Figure 2(b)

Figure 2 (a) and (b) the wafer box and vacuum pen with different color for GaAs and silicon process, respectively.

Wavetek's engineering and operating team are also dedicated. In clean rooms, Wavetek and UMC employees wear gowns of different colors for company identification and working area distinguishing. Operation disciplines are also announced routinely in Fab. The ICPMS check on silicon wafer indicates no contamination issue.

Engineers and operators performing operation and maintenance are well-educated on material property and toxicology. Because of the relative fragility of GaAs wafers when compared to silicon wafers, there is a SOP which engineers and operators are trained to follow the SOP. Robots are also calibrated to prevent broken wafers. Our current production line yield can achieve above 97%.

- **Separated MES Operation System**

In order to avoid mixing with Fab6A silicon operation, Wavetek owns operation and management system ourselves for in-line GaAs wafer processing. Figures 3(a) and (b) show the independent MES and operating management system, respectively. With dedicated engineering and operating team, mis-operation is prevented.

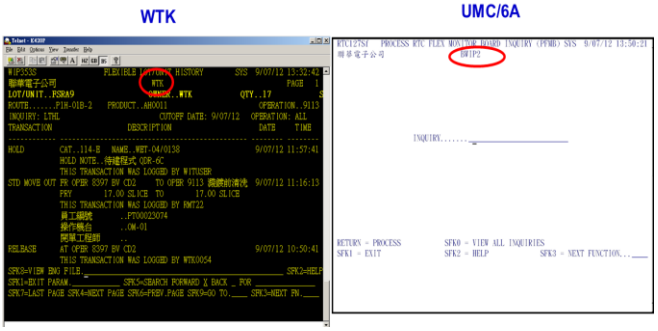


Figure 3 (a)

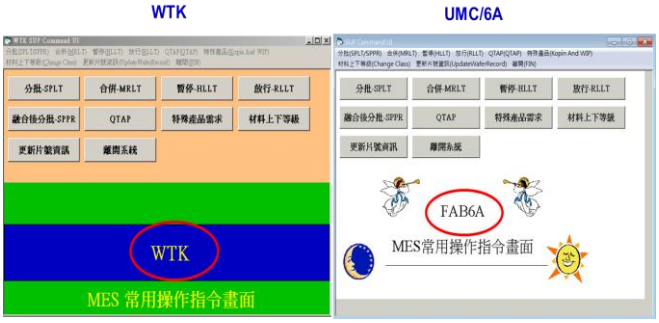


Figure 3 (b)

Figure 3 (a) and (b) the independent MES and operation management system for Wavetek and 6A, respectively.

Compared to silicon based MES, the additional step of Au recycling during manufacturing is required and important due to expensive material cost. A computerized system was developed to collect Au consumption data from several stages of manufacturing, including warehouse, fab stock, machine chamber and parts. Fab managers can monitor Au consumption rate and forecast recycle rate from the predefined formula in real time. Figure 4 illustrates the Au consumption monitoring in MES.

We are planning to develop an automated tool data collection system for Au consumption data feedback. The Au consumption rate is calculated per wafer run. With this system, Au residue in solution waste is greatly reduced and the recycle rate is enhanced to improve production cost efficiency.

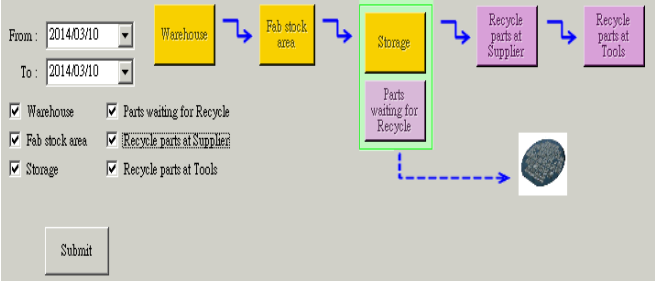


Figure 4 Au usage and consumption status monitoring in MES

Additionally, the facility system is monitored by the government environment agency and follows government's supply and waste disposition regulations.

- **GaAs Technology in Wavetek**

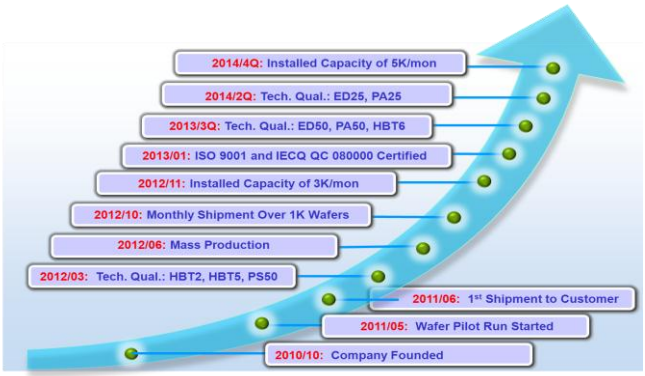
Our processes were initially licensed and transferred from GCS. These processes are high linearity and high saturation power HBT, and RF switch pHEMT. Our technology development team members have GaAs experience and a silicon foundry background, which speeds up the technology qualification although migrating wafer size from 4 to 6-inch. Equipment and tools were benchmarked with industry experiences and either retrofitted from silicon process or new purchases as described previously.

Our process qualification proceeds based on the industry standards before process releasing for mass production. Table 1 lists typical qualification items for a new process release.

Figure 5 shows our corporate major milestones. Within nine months, we completed the transferred process qualification and started mass production.

Category	Test Items	Test Standard and condition	Failure Criteria
Life Test	High temp operating life	JEDEC JEP118,	Determine the effect of temp and bias on device to get activation energy and MTTF 1. D Idmax, D b > 20% (pHEMT, HBT)
Environment	Biased HAST	JESD22-A110-B, 1.1xVdd 130℃, 85% RH, 2.26 atm, 96 hrs	Determine the effect of temp and humidity on the device under bias 1. D Idmax, D b > 10% (pHEMT, HBT) 2. Visual inspect w/o moisture penetrate
	Temperature Cycling Test (TCT)	JESD22-A104 Cond. C, -65℃ to +150℃, 500 cycles	Determine the effect of temp on material thermal mismatch 1. D Idmax, D b > 10% (pHEMT, HBT) 2. Visual inspect w/o swelling, dent, peeling
MIM Cap	TDDB	Voltage ramp test	0.1% failure @ 9V < 1E6 hrs
ESD	HBM ESD	MIL-STD-883E methods 3015.7	Determine the sensitivity of device to the level of ESD. Voltage shift over ±30% at I_{ref} of 1mA
	MM ESD	MM PER JESD22-A115	

Table 1 Wavetek's qualification plan for a new process release



. Figure 5 the corporate major milestone of technology set-up

- **Summary of Wavetek GaAs Technology**

As a pure-play GaAs foundry, our mission is to provide comprehensive and healthy processes meeting customers' product application requirements in wireless communication areas. We have dedicated R&D teams to develop more processes, such as HBT and ED-pHEMT for higher PAE/linearity performance, 2G/Edge/TD combo PA, and infrastructure applications. These processes are all qualified as shown in Table 1.

Parameters	Unit	HBT2	HBT3	HBT5
Application		W-CDMA, WiFi (802.11 a/b/g/n/ac), LTE, Gain Block.	MMMB (Multi-Mode-Multi-Band), GSM/EDGE Combo, GSM/EDGE/ TD-SCDMA Combo.	GSM, HV gain block.
DC Current gain (Beta)		70	75	70
BVceo	V	14	16.5	18.5
BVcbo	V	25	27	33
f_T	GHz	40	35	32
f_{Max}	GHz	58	58	60

Table 2 Wavetek's HBT Portfolio

The fabrication process is the same among all HBT processes. The only difference is Epi structure for different applications. Table 2 shows the characteristics of our HBT offering. Table 3 shows the characteristics of our pHEMT process. Both ADS and Cadence PDK are provided for customer's design and layout verification. Furthermore, the customization or porting process can also be implemented through project collaboration or joint development.

Parameters	Unit	PS_50	ED_50		ED_25		PA_50	PA_25
Applications		LNA/Switch for WCDMA, WiFi(802.11 a/b/g/n/ac), LTE, GPS.	LNA/Gain Block/ Switch for WCDMA, WiFi(802.11a/b/g/n/ac), LTE, GPS.		LNA/Gain Block/ Switch for WCDMA, WiFi(802.11a/b/g/n/ac), LTE / GPS.		Gain Block/ Power Amplifier for 2-20 GHz (X/Ku bands)	Gain Block/ Power Amplifier for 20-80 GHz (K/Ka/V/W bands)
Device Type		D-mode	E-mode	D-mode	E-mode	D-mode	D-mode	D-mode
Vth / Vp	V	-1	0.25	-1	0.3	-1	-1	-1
IDSS	mA/mm	266	1.0E-04	270	1.0E-04	320	300	320
GM	mS/mm	350	550	350	850	450	350	450
VBDG	V	15	15	15	12	15	20	18
Ron	Ohm · mm	1.6	1.8	1.6	1.2	1	-	-
NF	dB	0.9 at 6GHz	0.7 (at 6GHz)	-	0.3 (at 6GHz)	-	0.9 (at 10GHz)	0.6 (at 10GHz)
ft	GHz	33	33	33	70	60	33	60
fmax	GHz	90	100	90	120	100	90	200

Table 3 Wavetek's pHEMT Portfolio

Conclusions

In summary, Wavetek team is built with a group of experienced GaAs and silicon foundry experts to provide pure-play GaAs foundry service. We offer various robust processes, IP service, and competitive cost structure in wireless communication product applications.

With a dedicated team, tools, and demanding manufacturing discipline, it is proven that GaAs and silicon wafers can be processed in the same Fab without cross contamination.

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Acronyms:
GaAs: Gallium Arsenide
MMIC: Monolithic Microwave Integrated Circuits
CMOS: Complementary Metal-Oxide Semiconductor
HBT: Heterojunction Bipolar Transistors
pHEMT: Pseudomorphic High Electron Mobility Transistors
MES: Manufacturing Execution System
ICPMS: Inductively Coupled Plasma mass Spectrometry
SOP: standard of operating