Effect of Multi-Field Plates on the Reverse Breakdown and Leakage Characteristics of GaN-on-Silicon HEMTs

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Abstract
MACOM Technology Solutions has a continuing joint development efforts sponsored by the Department of Energy with MIT main campus and MIT Lincoln Laboratory to develop GaN on silicon three terminal high voltage/high current switching devices. The initial developmental goals were for a three terminal structure that has a reverse breakdown characteristic of >1200 volts and is capable of switching 10 amperes of current, with a current breakdown target of 3000 volts. This paper presents an update on the progress of this multi-year development project against these on-state current handling, reverse leakage and breakdown goals.

INTRODUCTION
As reported by the authors at CS MANTECH in 2013¹, an individual breakdown on a single finger 250 μm GaN-on-silicon HEMT device with a SCFP of >1630 volts at a current of 250 μA (1 mA/mm) was achieved. Also, over 5.5 amperes of Iₘₐₓ current utilizing a HEMT structure without a SCFP and having 10 mm of gate periphery, corresponding to a normalized current handling of at least 550 mA/mm was observed and an Iₘₐₓ of 4.5 amperes and a normalized current density of 450 mA/mm was realized on a identical transistor geometry but with the addition of a SCFP.

While these results were clearly more than competitive when compared to findings reported in the literature and industry, see Figure 1, it was clear that in order to both improve the reverse breakdown characteristic and have the ability to produce a practical HEMT for high voltage switching applications, the baseline leakage needed to be reduced significantly.

DISCUSSION
A study of the basic tunnelling mechanisms that dominate the leakage characteristics of GaN Schottky diode electrodes was undertaken. The results of this investigation have been published¹. It was found that Frenkel–Poole (FP) trap-assisted emission and Fowler-Nordheim (FN) tunnelling are the two overriding sources of leakage in GaN Schottky electrodes. Further, each of these mechanisms governs the reverse Schottky junction in different electric field regimes, as shown in Figure 2. Also, as seen in Figure 2, FN tunnelling is temperature independent, and is the dominant leakage mechanism for electric field values >1.6 MV/cm. Thus, in order to control the high voltage leakage and reverse breakdown characteristic, it is critical to properly
engineer the spreading of reverse electric field by means of proper field plate design.

Extensive modeling studies on the design of stem slope, gate connected, and source connected field plates and corresponding dielectric thickness have been completed for single, double, and triple field plate structures. This modeling optimization utilized a 2-D structure simulator from Silvaco to analyze the effect of the field plate overlap on the drain side of the gate, the dielectric thickness and dielectric constant, the total number of field plates required, and the specific transistor terminal connections. The device simulator predicted that the peak electric fields occur, both in the GaN channel and the AlGaN barrier layer, adjacent to the gate on the drain side of the HEMT transistor, at the edge of the GCFP field plate, and at the edge of the SCFP. Since there are multiple peak electric fields in these various field plate configurations, to maximize device reverse breakdown the goal is to optimize the field plate structures to maintain all of the peak electric fields below 3.0x10^6 V/cm, the theoretical field strength limit for gallium nitride.

**RESULTS**

Based upon this structure modeling, a HEMT test reticle was designed. A screen capture of the final layout is shown in Figure 3. It can be seen that this multi-field plate test reticle consists of 152 single gate variants with non-field plated devices as controls; source connected field plated (SCFP) structures of various overlap dimensions; gate connected field plated (GCFP) configurations of different overlap dimensions; combined multi-field plate designs with dual source connected and gate connected field plated configurations. In addition, multiple gate-to-drain spacings ranging from 5 μm to 20 μm were considered to support the total applied reverse field. The goal of these field plate variants is to spread and reduce the peak fields at the drain side edge of the gate; the edge of the GCFP; and the edge of SCFP. In addition, there are 24 variants of high current, multi-gate HEMT transistors having a total of 20 mm of gate periphery. These multi-gate devices are a mixture of SCFP, GCFP, and dual SCFP&GCFP structures and having fixed 10 μm gate-to-drain spacings.

![Screen Capture of HEMT Multi-Field Plated Test Matrix](image)

![Single Gate HEMT Device with a Dual GCFP and SCFP Field Plate](image)
from the edge of the respective field plate to the drain contact. By adding the indicated field plate-to-drain contact spacing the corresponding field plate overlap spacing, it can be seen that for the single gate example, the gate-to-drain feature is 10 \( \mu \text{m} \) in length. Lastly, it can be seen that the spacing between the probe pads is a minimum of 400 \( \mu \text{m} \) in order to prevent arcing between the probe tips during on wafer characterization.

Several lots of this multi-field plated design were initiated into the wafer fab utilizing wafer splits of epitaxial materials having a range of 12.4 nm to 18.0 nm thick Schottky barrier active layers to reduce the sheet charge in the 2DEG conduction layer. In addition, both P+ doped, CZ silicon substrates with a 4.8 \( \mu \text{m} \) thick AlGaN buffer layer, and high resistivity FZ silicon substrates with a 2.6 \( \mu \text{m} \) thick buffer layer were employed to minimize vertical, ohmic-to-ohmic buffer leakage through the substrate.

Test results for one wafer from the latest experimental lot are presented in Figure 5 through Figure 8. This wafer had a high resistivity, FZ silicon substrate with a 2.6 \( \mu \text{m} \) thick AlGaN buffer layer and a Schottky barrier active layer that was 18.0 nm in thickness. Of the 152 single gate designs, data for six units from each of six specific devices, which utilized variants that encompassed a non-field plate HEMT structure, a single SCFP only configuration, two different GCFP only constructions, and two designs with different combinations of a GCFP, and a SCFP with different SCFP/GCFP drain overlap dimensions and field plate offsets, have been plotted. All of the above device options utilized a gate stem sloped field plate, and a gate to drain spacing of 20 \( \mu \text{m} \). Additionally, the data for the six units of each design modification was taken as an across wafer map to provide information on the wafer breakdown distribution.

It can be seen in Figure 5 that the six non-field plate structures generally had very high initial, low voltage baseline leakage, in the 1.0x10\(^{-3}\) to 1.0x10\(^{-4}\) ampere range, and exhibited a significant drop in reverse leakage as the reverse bias was increased to approximately 200 volts. As can be seen, as additional reverse voltage was applied the baseline level decreased dramatically to the resolution limit of the tester, 1.0x10\(^{-11}\) to 1.0x10\(^{-12}\) ampere, which is indicative of trapping sites within the drain of the HEMT structure being filled. As the reverse stress is further increased, reverse breakdown can be seen to occur in the 300 volt to 400 volt range with one unit as high as 800 volts. This variation in leakage level and wide discrepancy in voltage breakdown was observed to vary positional across the wafer and is exactly what has been seen and described previously in the development project as center-to-edge variation.

In Figure 6, data for six devices of a SCFP only GaN-on-silicon HEMT design is compared to the non-field plate data that was shown in Figure 5. It can be seen that all six units had low voltage baseline leakage that was at the tester compliance limit of 1.0x10\(^{-11}\) to 1.0x10\(^{-12}\) amperes, a similar wide variation in reverse breakdown voltage is observed, with a low reading of 500 volts, ranging to two devices at 1100 volts, and several devices at the auto-tester voltage compliance limit of 1200 volts. While this is a significant improvement over the non-field plate designs, an across wafer deviation in breakdown voltage is still present.

Two different GFCP only designs which had different drain overlap dimensions were measured. As shown in Figure 7, which contrasts these GCFP only designs relative to the standard non-field plated GaN-on-silicon HEMT structure, it can be seen that both GCFP only approaches, in a similar manner as that of the SCFP only variant presented in Figure 6, had low voltage baseline leakage at the low level limit of the tester, 1.0x10\(^{-11}\) to 1.0x10\(^{-12}\) amperes. It can be seen that all six units of the GCFP only design with a 1.5 \( \mu \text{m} \) drain overlap dimension maintained this baseline leakage level out to the voltage 1200 volt tester limit. The
second GCFP only design, but with a 3.0 \( \mu \)m drain overlap dimension, fared almost as well. In this case, four of the six units were identical to the smaller GFCP overlap design with the remaining two devices reaching reverse breakdown between 900 volts and 1000 volts.

Lastly, it can be observed in Figure 8 that for the dual GCFP/SCFP designs, all twelve measured units, regardless of the specific field plate geometries, reached the on-wafer auto-tester voltage limit of 1200 volts before avalanche breakdown was achieved. It can also be seen that all of the twelve devices, again with a similar insensitivity to the field plate layout, had a baseline leakage of less than \( 1.0 \times 10^{-11} \) amperes, again limited by the low level leakage compliance on the auto-tester. Since these single gate HEMT devices have a gate periphery of 250 \( \mu \)m, this low level leakage normalizes to a current level of \( 4.0 \times 10^{-8} \) mA/mm of gate periphery. This very low reverse baseline leakage current contrasts dramatically with the leakage floor of approximately \( 1.0 \times 10^{-3} \) mA/mm that was observed previously\(^1\), a five order of magnitude improvement in gate-to-drain leakage. In addition, the across wafer breakdown non-uniformity which generally followed a center-to-edge pattern and has been an issue throughout the early phases of this developmental effort, has been completely eliminated.

CONCLUSIONS

A study was performed to understand the fundamental behavior of tunneling currents in GaN Schottky electrodes. Two dimensional simulations were performed on gate stem sloped field plates, GCFP, SCFP, and multi-field plate geometries to spread and reduce the peak fields at the edge of the gate and the edges of the field plates. Based upon the fundamental studies and the 2-D structure simulations, a three terminal evaluation mask was designed having a series of single finger HEMT structures to validate the effect of the field plate variants and the gate to drain spacing on the reverse leakage and breakdown performance. An average three terminal breakdown of 1200 volts was measured on a single finger 250 \( \mu \)m GaN-on-silicon HEMT devices utilizing multi-field plate geometries, sloped stem FP/GCFP/SCFP geometries. Even more impressive is the observed \( 10^5 \) times improvement in the HEMT reverse leakage current which validates the modeling of the fundamental tunneling leakage mechanisms enabling further high voltage reverse breakdown improvement.

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REFERENCES


ACRONYMS

GaN: Gallium Nitride
SiC: Silicon Carbide
AlGaN: Aluminum Gallium Nitride
HEMT: High Electron Mobility Transistor
GCFP: Gate Connected Field Plate
SCFP: Source Connected Field Plate
FZ: Float Zone
CZ: Czochralski