A Mathematical Model to Determine the Impact of Through-Wafer-Vias on Backside Plating Thickness

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Abstract

While through-wafer-vias (TWVs) etched into the backside of semiconductor wafers appear to be very small, their combined surface area can have a significant impact on backside plated metal thickness. This paper introduces a model that can estimate plating thickness changes based on via geometry and the total number of vias etched in a wafer. The model recommends process changes to successfully match plating thickness across products with different mask designs.

INTRODUCTION

As part of a continuous process improvement effort, we wanted to tighten control of our backside plating thickness at our GaAs wafer manufacturing facilities in Newbury Park, California. This process electroplates several microns of copper on a thin gold and nickel-vanadium film that acts as a copper diffusion barrier. There is no mask pattern on the wafer during plating; the entire backside and etched through-wafer-vias are plated as a single sheet film.

One would expect that plating relatively flat surfaces results in consistent plating thicknesses from one wafer to the next. Likewise, plating thicknesses should be very close across different products.

However, we noticed that plating thicknesses fell into distinct product groups as inferred by measuring the sheet resistance (R_s) of the plated film. When the sheet resistance shifted, it generally shifted for all groups together, which indicated that the differences among products were independent of process variation attributed to plating bath and equipment parameter changes (see Figure 1). The main difference among products was the number of vias on the wafer. Some had many tens of thousands of vias, and others had several hundreds of thousands. Surely this difference in the number of these tiny vias could not be the reason for these plating thickness differences, or could it?

A newly developed model revealed that not only the number of vias but also via dimensions, via surface roughness, and wafer thickness all have a significant effect on backside plating thickness because of their collective impact on total wafer surface area. By incorporating these factors into the model, we could now evaluate the impact of each factor independently and determine what adjustment to plating time is necessary to compensate for differences in plating thickness across different products.

DETERMINING THE MODEL INPUT VARIABLES

EXISTING VIA DIMENSIONS

In a cross section profile our vias have a wineglass shape: (See Figure 2).

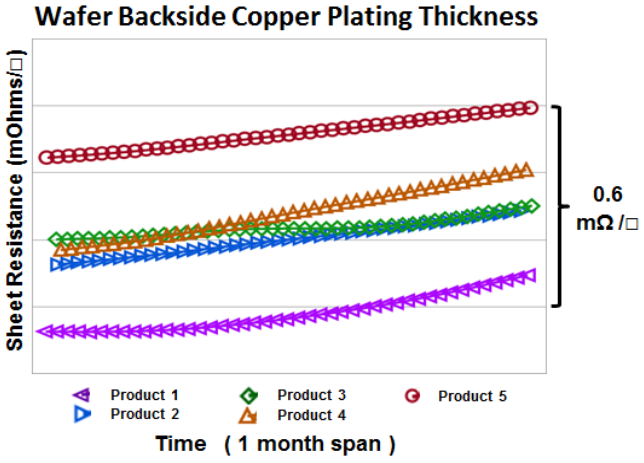


Figure 1: R_s of Backside Plated Copper vs. Time by Product

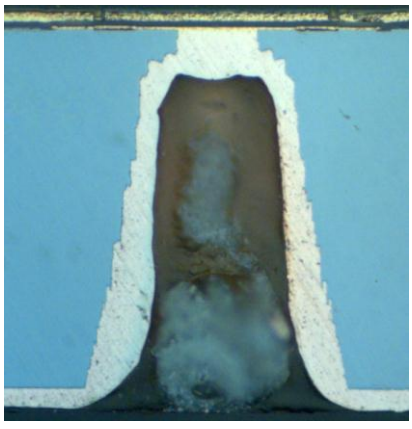


Figure 2: Cross Section Profile of Via Filled with Plated Metal

The via shape is defined by the photoresist pattern and via etch process steps. The photomask uses a rectangular opening in the chrome plate to define each via. After exposure on a relatively low resolution contact aligner and develop, the rectangle pattern in the resist has rounded corners. Next a bake step heats the resist to remove residual solvent and to improve adhesion, causing the vertical via profile to change. The top of resist contracts as solvent diffuses out from the bulk resist material but the bottom of the resist is pinned by its adhesion to the substrate. At the end of the bake the resist profile is sloped at the top of the via opening.

During the via etch step gases remove the GaAs substrate material everywhere the photoresist does not mask them. The etch creates holes in the substrate with near vertical walls. With longer etch time the resist slowly erodes at the bottom of the via where the resist is the thinnest. The via opening increases in size allowing the etch gases to widen the etched hole dimension. Etching continues until the recipe detects the reduction in etch byproduct material at the bottom of the via as tuned by the process engineer to coincide with the desired length and width of the designed via dimensions. This gradual resist erosion and hole widening shifts the vertical via profile to a sloped via profile.

The surface profile and via dimensions are needed so that the model can estimate the surface area of a via. With one via modeled, the total surface area of the wafer is just the sum of the surface area of all vias and the surface area of the back of the wafer excluding via openings.

Starting at Square One With a Rectangle

The model starts with the assumption that a via is a perfect rectangle. It assumes the final etched via wall profile is linear and the top is larger than the bottom (see Fig 3).

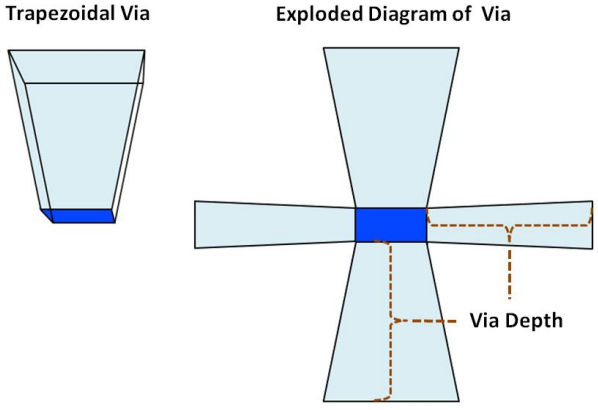


Figure 3: The Via Model Starts with A Trapezoidal Prism

The top and bottom rectangle dimensions are determined based on actual wafer measurements using a focused ion beam scanning electron microscope (FIB SEM), and the wafer thickness is the height of the prism. The area of the sidewalls and bottom of this prism are now a rough estimate of the surface area of one via.

The first correction to the model changes the shape of the via opening from a rectangle to an ellipse. The ratio of the perimeter of the ellipse to the perimeter of a rectangle is used as a correction factor to the surface area of the bottom of the via. If we assume the via shape does not change significantly from the bottom to the top of the via, the perimeter ratio can be multiplied by the total surface area of the via walls of a rectangular via to determine the surface area of the elliptical via. This mathematical trick allows us to bypass the need to incorporate the slope of the elliptical via into the calculations since the slope is already included for the rectangular via calculations.

A further correction changes the ellipse to more closely match the actual via shape which resembles a rectangle with rounded corners (see Figure 4). This adjustment is somewhat subjective based on observations of vias on wafers after they have been etched.

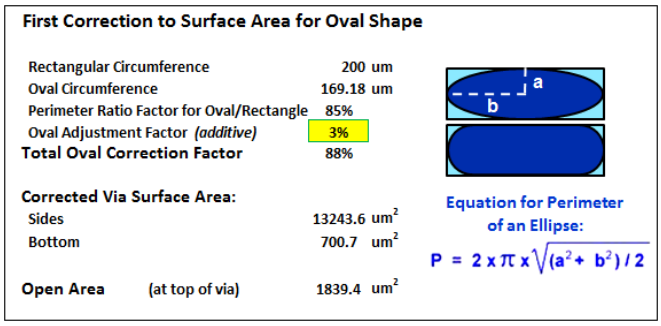


Figure 4: Elliptical and Oval Corrections to the Rectangular Via Model

Plating Volume Inside A Via

Since via openings are very deep and narrow, metal ions in the plating bath reach and plate the top of the via quickly while other ions take longer to diffuse toward the bottom of the via. The plating thicknesses at the bottom of the via tends to be only a fraction of thickness on the back of the wafer. However if the sidewall thickness is estimated as a linear change from the top of the via to the bottom, the model can use the average thickness as the estimate. Plating thickness measurements are taken from FIB SEM cross sections.

These estimates of the plating thickness at the bottom and sidewalls of the via are applied as the second correction factor in the model (see Fig 5).

The thickness estimate of the sidewall multiplied by the via surface area generates the volume of plating for the via sidewalls. The plating thickness at the via floor is multiplied by the bottom rounded rectangular area to determine the plating volume at the base of the via. Combining both of these volumetric results establishes the first estimate of the plated metal volume inside one via.

Second Adjustment for Plating Thickness Change Inside Vias

Average Thickness on sidewall (um)	2.5	1/2*(Top + Bottom)
Adjustment for Thickness change on sidewall	83%	1/2*(Top + Bottom) / Tgt Thk
Thickness Ratio at Bottom of Via (um)	50%	(Bottom/Top)

		Corrected Surface Area:
Calculation reduces actual surface area to simulate reduced plating thickness.	Sides	11036.3 um^2
	Bottom	350.4 um^2

(i.e.: If plating thickness is 1/2 targeted thickness, effective surface area is simulated as 1/2.

Figure 5: Correction Factor for Plating Thickness Change Inside Vias

BACKSIDE PLATING VOLUME

The backside plating volume is determined by subtracting the surface area of all via openings (the holes) from the backside wafer area and multiplying it by the plating thickness measured in wafer cross sections.

Multiplying the total number of vias on a wafer by the plating volume of one via and adding this to the backside plating volume equates to the first order estimate of plating volume for the wafer.

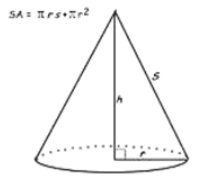
So far the model assumes all plated surfaces are smooth. Roughness due to minor surface contamination as well as spikes on via walls can add considerable plating surface area. However, the model does not need to apply roughness estimates to the backside wafer surface, because this surface is common to all products. Therefore, the only location where roughness on plating surface area would be different is the sidewalls of the vias.

To address surface roughness in vias the model uses a third correction factor. A spike or particle on the sidewall can be simulated by the surface area of only the top of a cone (See Figure 6).

Third Correction to Evaluate Roughness Inside Vias

(applied only to via sidewall surface area, not bottom of via or wafer backside)

Estimate the average height of all pillars and spikes in the side wall surface:



Surface area = $\pi r \sqrt{r^2 + h^2}$

Height	1	um
Base diameter	0.5	um
Cone side length	1.031	um
Base area	0.196	um^2
Bump Surface Area	0.810	um^2
Bump density	50%	
Roughness factor =	2.06	

When exposed pillars are hollow this estimate would be too low

Exposed spikes may have a higher charge density and may cause localized thicker plating

Figure 6: Correction for Surface Roughness using Cone Structures

The average height of spikes and steps on via walls as seen in FIB cross section photos is used to estimate the cone height. The density of spikes is estimated by evaluating the average distance between spikes in the sidewall. This correction factor is determined by taking the ratio of surface area of a bump (the cone) vs. the surface area no bump (a circle) multiplied by the density estimate and the total number of vias on the wafer.

ESTIMATING PLATING THICKNESS AND PLATING TIMES

After applying these correction factors the model is calibrated by collecting sheet resistance data from unplated wafers, plated wafers with no vias, and wafers with known numbers of vias. Plating thickness is inferred from the sheet resistance data using the equation:

$$\text{Plated Cu Thk} = \frac{\rho + \Delta}{1 / (1/R_{s\,(\text{Plated Film})} - 1/R_{s\,(\text{Seed})})} \quad (1)$$

where ρ is the resistivity of the plated metal and Δ is a very small correction factor used to match the actual and theoretical resistances. The four point probe tool is calibrated to ANSI resistance standards in the range of resistance measurements used by production and test wafers, and successfully passed a Gauge Repeatability and Reproducibility (GR&R) test completed over several days by several technicians.

The plot of the sheet resistance data from plated wafers with varying numbers of vias is shown in Figure 7:

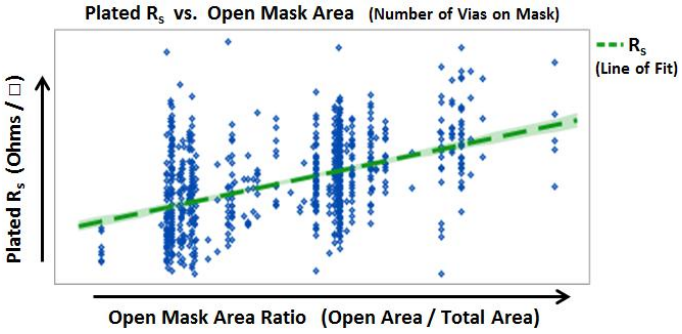


Figure 7: Plated Sheet Resistance vs. Open Mask Area Ratio

The open mask area ratio is a parameter calculated by the mask design software. It totals all exposed mask area and divides it by the total available mask area. This ratio correlates to the total number of vias on each product design. As the number of vias increases, the open mask area increases. Figure 7 shows that when the number of vias on a product increases the plated sheet resistance also increases.

Since wafers of different products were plated on the same equipment close in time, all other process factors during plating were fairly equal. Therefore, differences in plating thicknesses not only *correlated* to the number of vias on the wafer but they were *the cause* of the plating thickness changes.

This conclusion allowed us to start to compensate plating thicknesses by adjusting plating times. Since R_s decreases linearly with plating time, it was possible to assign plating times to each product by comparing the R_s result to a reference product with a known number of vias and a fixed plating time. Based on this calculation the model could recommend a correction to plating time as compared to the reference product when R_s results were higher or lower than expected.

Rather than maintaining hundreds of recipes with different plating times optimized for each product, we chose to combine products into groups based on the number of vias for each product. Each group was assigned one of five plating recipes with plating times adjusted to minimize group-to-group thickness variation. The plating time difference between groups was around 5%. With five plating groups the difference between the highest and lowest groups was near 20%.

Sheet resistance data collected on thousands of plated wafers using many products with significantly different number of vias allowed us to fine tune original subjective correction factors, such as the oval adjustment factor and wafer roughness adjustment factor. Implementing these plating time changes resulted in > 50% reduction in wafer to wafer backside copper thickness variation across all products (See Figure 8).

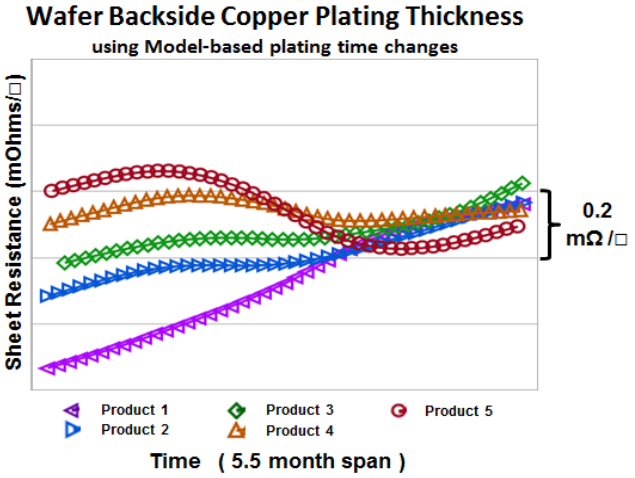


Figure 8: R_s of Plated Copper over Five and a Half Months using Model-based Plating Time Changes

Plating time selection has been automated so that new products automatically get the correct plating time based on the open mask area defined by the mask design. One of five plating recipes is selected depending on which of the five bins the open mask area falls into when the product is first introduced into manufacturing.

CONCLUSION

Plating thickness variation is not just a function of process and equipment variation. For through-wafer-vias the mask design also has a significant impact. Plating thickness is affected by the total surface area on the wafer, including the plating surface area inside TWVs, previously considered to have a negligible impact. Experimental data revealed that different products receiving the same plating time had signficantly different backside plating thicknesses and that these differences were not related to process or equipment parameter drift.

It is now possible to estimate plating thickness differences across different products using a model that collects inputs of wafer thickness, number of vias on the wafer, via shape, plating thickness profile, via roughness, and plating time. The model is calibrated by collecting plated thickness measurements and sheet resistance data from product wafers with a known numbers of vias. The model uses open mask area data calculated from the mask design software to translate an expected difference in sheet resistance into a recommended plating time change. After the plating time adjustment was applied on thousands of wafers from different products, we achieved more than a 50% reduction in backside plating thickness variation across all products.

ACRONYMS

TWV	Through-Wafer-Via
R_s	Sheet Resistance
FIB	Focused Ion Beam
SEM	Scanning Electron Microscope
GR&R	Gauge Repeatability and Reproducibility

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