A new approach for GaN normally-off power transistors: Lateral recess for positive threshold voltage

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Abstract
We present a new approach for normally-off transistors based on a recess leading to a laterally induced positive threshold voltage. The fabrication process is demonstrated to yield devices with positive threshold voltage. The breakdown voltage of these devices compares well with that of equivalent normally-on devices. Future work is directed towards passivation of the devices in order to reduce the impact of surface traps on device properties.

INTRODUCTION
The power switching market for the automotive and transport industry, consumer and household electronics, manufacturing as well as energy generation, distribution and storage is rapidly increasing. Future systems will require transistors fabricated from nitride semiconductors in order to decrease volume, weight and cooling needs as well as to increase the overall efficiency. From a safety point of view it is highly desirable to use enhancement mode devices as these automatically turn-off in case of a failure in contrast to their depletion mode counterparts.

GaN-based transistors are in general lateral devices that use the polarization-induced two-dimensional electron gas (2DEG) for electron transport which is modulated by a gate contact in between the source and drain contacts. The sheet carrier density increases with both the thickness and the Al-content in the AlGaN/GaN heterostructure that is grown on top of a buffer layer. Hence, transistors fabricated from this materials system are usually normally-on devices.

In order to realize GaN-based normally-off transistors so far special plasma treatments [1], p-type layers underneath the gate contact [2] or a gate recess under the gate contact [3] have been pursued. These approaches have demonstrated normally-off devices but suffer from tight technological windows (epitaxy and processing) and complexities that complicate a reproducible fabrication of such normally-off devices. Plasma treatments require very elaborate optimization steps and thus cannot easily be transferred to different toolset, hence making them not suitable for production. P-type layers and a gate recess underneath the gate require a very precise control of the removal procedures

Figure 1: Schematic fabrication and operation principle of the presented normally-off transistors using a single (upper images) and double (lower images) gate contact. (a) The process starts with a planar semiconductor surface, source and drain ohmic contacts as well as an insulated gate contact. (b) A resist mask is used to define the area for the dry etch with the gates used as additional hard mask to define the dry etch into the semiconductor (removing the barrier partially or completely or even removing part of the GaN buffer), thus interrupting the 2DEG and leading to a blocking at zero gate bias. (c) Once a positive bias is applied to the gate charge is accumulated until the gate bias is large enough to allow a current from source to drain.
in the access region and below the ohmic contacts respectively under the gate contact.

IDEA FOR NORMALLY-OFF

Here, we propose a new approach for nitride semiconductor normally-off transistors that is based on a recess etch in the source gate region in order to realize a positive threshold voltage with reduced technological complexity, see Figure 1. The process distinguished itself by a stable technological route for shifting the threshold voltage of a transistor. Starting point is a standard epitaxial and technological structure for normally-on devices having a continuous 2DEG between source and drain with an insulated gate using a dielectric layer between semiconductor and gate metal.

The normally-off behavior is achieved using a recess etch of sufficient depth on the source-side of the gate, thus interrupting the 2DEG between source and gate. At zero gate bias there is no current flowing between source and drain for applied drain bias. Driving the gate contact into positive bias leads to carrier accumulation underneath the gate region and finally a current is flowing from source to drain once the gate voltage is large enough. Optionally the recess is performed between two gate contacts (see Figure 1b) and carrier accumulation is performed utilizing the two gate contacts. In both cases a combination of a resist mask and the gate contacts as hard mask is employed for lateral definition of the recess.

For the lateral control of the recess with the self-aligned approach with two gate contacts is preferable as the recess width is defined in a single lithography step whereas the approach with a single gate and a resist layer relies on the alignment accuracy between these two layers.

FABRICATION PROCESS

We have realized such normally-off devices (see Figure 2) using standard epitaxial layers on 3-inch semi...
Furthermore, with increasing lateral dimensions we observe a drop in maximum current density which we attribute to high surface state density of the unpassivated recess area.

We have tested the reproducibility of our process by repeating the experiment with an etching time of 40 s for gate dielectric and semiconductor layer. The result is promising as the resulting threshold voltage is within 100 mV for three repeated wafers.

In order to investigate the high voltage robustness of our samples we have carried out breakdown measurements, see Figure 3c. For these measurements the gate bias was zero, the measurements itself were carried out in FC-43 liquid in order to prevent breakdown through air. Up to the device failure induced breakdown voltage of around 700 V the leakage currents are below $10^{-8}$ A (50 µm gate width) demonstrating the high voltage stability of the structures. The breakdown voltage is in good agreement with normally-on devices having Schottky gates with the same gate-to-drain distance.

Output current-voltage curves of the proposed normally-off transistors are given in Figure 4, indicating that the on-state decreases as expected with increasing gate bias. For a fixed gate bias the on-state resistance is stable up to the knee-voltage.

**SUMMARY AND CONCLUSIONS**

In summary we have presented and experimentally verified a new approach for normally-off transistors based on a recess leading to a laterally induced positive threshold voltage. Future work is directed towards passivation of the devices in order to reduce the impact of surface traps on device properties.

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**REFERENCES**


**ACRONYMS**

HEMT: High Electron Mobility Transistor
MOCVD: Metal Organic Chemical Vapor Deposition
2DEG: Two-Dimensional Electron Gas