Improved GaAs HBT Device Linearity with Flattened Cutoff Frequency Curve

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Abstract

Modern communications require high linearity for power amplifiers. GaAs heterojunction bipolar transistor (HBT) based amplifiers are proven to have high efficiency, good linearity, ruggedness, and low cost. In this paper we report on an improved linearity GaAs HBT device achieved through a novel engineered Ft curve. The novelty of the solution relies on the flatness of the Ft curve with device current density.

INTRODUCTION

InGaP/GaAs heterojunction bipolar transistors (HBT) are widely used for wireless applications since they offer excellent features such as high power density and high efficiency. In addition, for many analog applications, the device linearity is paramount. This feature is best described by the intermodulation distortion, which is a key circuit parameter for these RF applications.

The intermodulation distortion (IM), and hence device linearity, is well known to be caused by three major components from the HBT structure: (1) the transconductance (gm), (2) the base-collector capacitance (Cbc), and (3) the transit time.[1,2] In this paper we will focus on the less experimentally investigated concept, that of the influence of the cutoff frequency (Ft) curve versus device current density flatness and its influence on device linearity (transit time non-linearity).

DEVICE LINEARITY ENHANCEMENT METHODS

Most of the device linearity studies have been focused on the variation of Cbc depending on the bias conditions,[3] the input signal, and the collector epitaxial structure.[4] The Cbc variation is less significant if both the doping and thickness of the collector are low, so that the collector is fully depleted at low voltage. However, the resulting device breakdown voltage is low and not suited for current PA applications which require voltages up to 20V. As a consequence, alternate collector doping profiles were employed to maximize the breakdown voltage while maintaining the collector thickness and power capabilities of the device. Such profiles used either (1) doping spikes,[5] a thin higher doping layer placed somewhere within the uniformly doped collector, (2) step-graded collectors, and (3) collector doping ramps.[6,7]

The first method consists in the introduction of a highly doped, sharp, n-type spike in the lower doped collector. This is designed just so that the collector depletion layer is limited by the doping spike under normal operating bias. This depletion length will be pinned at this position and the device behaves like a punched through HBT which results in a lower Cbc variation and thus better linearity. When the collector voltage is highly increased, the doping spike will be fully depleted and the depletion layer will extend into the lightly doped collector layer between the spike and the subcollector, giving the device better ruggedness. One limitation of this method is that the spike doped layer should be depleted before the breakdown voltage which limits the doping and thickness of the layer.

In our previous work on spike doped collector HBTs,[8] a structure with a doping spike of 2E18 cm^{-3} and thickness of 10 nm placed in the middle of a 1.1 µm thick collector with a uniform doping of 7.5E15 cm^{-3} resulted in no Cbc variation above approximately Vce = 2V and a delay in the Kirk effect onset coupled with an increase in cutoff frequency. A step-graded collector with the same flat doping in the collector region close to the base provided much less variation in Cbc but with a penalty in ruggedness. Overall, application of these HBT structures in actual power amplifier circuits did not result in improved linearity.

Collector doping profiles with either (1) uniform doping followed by a doping ramp, or (2) uniform doping followed by two regions of increasing doping ramps have been used to provide better ruggedness by increasing the device snap-back loci with device current.[6,7] This improvement is due to the increase in the current density required to trigger the avalanche injection, thus allowing the HBT to survive momentary overloads.

While the first method may generate more uniform Cbc profiles, all these methods enhance the device Ft at higher current densities, effectively delaying the onset of the Kirk effect. The delay of the Kirk effect has beneficial effects on the device linearity due to the lower curvature in the Ft curve within the operating range of the collector current.

DEVICE FIGURES OF MERIT

The devices used in this work were fabricated using Skyworks' standard InGaP HBT/BiFET process. The collector profile for the new devices was optimized by incorporating all these collector doping profile engineering

methods, i.e. doping spikes, step grading, and doping ramps to realize a more linear operation. Devices of various seizes were laid out as test structures in Ground-Signal-Ground pads and tested over a wide range of frequencies between 100 MHz and 6 GHz, at small signal, using an Agilent PNA, over bias points extending from Vce of 0V to 5V, and device current densities between about 0.008 mA/μm^2 and approximately 0.6 mA/μm^2. Following the measurements, the base-collector junction capacitance Cbc was extracted, together with other RF device figures of merit such as MAG/MSG at frequencies of interest and Ft.

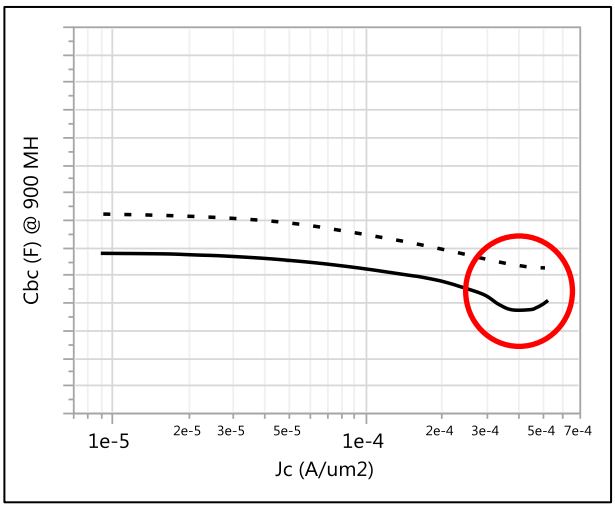


Figure 1. Extracted Cbc curve (arbitrary units, linear scale) versus device current density at Vce=1.5V, 900 MHz (dashed line is the improved structure).

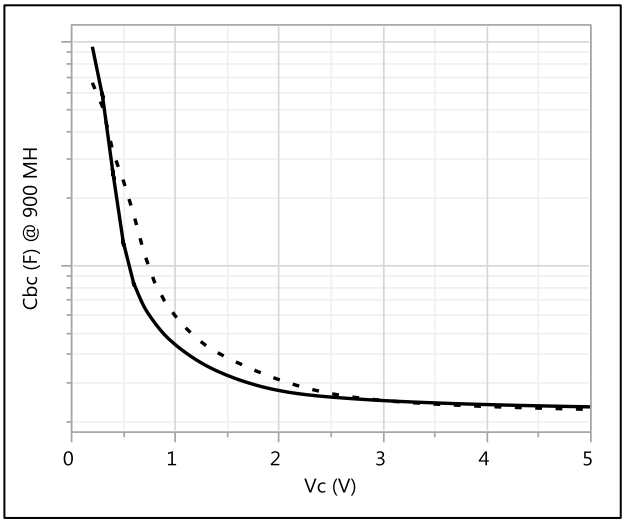


Figure 2. Extracted Cbc curve (arbitrary units, logarithmic scale) versus Vce at Jc=0.25 mA/μm^2, 900 MHz (dashed line is the improved structure).

Figure 1 shows the average extracted Cbc versus the collector current density at Vce=1.5V and a frequency of 900 MHz. Although the new epitaxial structure shows more than a 10% increase in capacitance compared to our linear epitaxial material (standard) so we can expect a small degradation in device RF gain, the capacitance variation across the current density range is lower, especially at higher current density. The same data is displayed in Figure 2, but this time versus Vce, at a current density of 0.25 mA/μm^2 to look at device saturation performance. The new structure has less Cbc overall with less curvature at lower voltages. Although some improvements in Cbc variation were noted, it is difficult to assess the effect on the device linearity.

Impact of Cutoff Frequency Curve Nonlinearity versus J_C on the Device Intermodulation Distortion

Rather than rely on the uniformity of the Cbc vs bias, one can seek the improvement of the device linearity (less intermodulation distortion) based on the behavior of the Ft curve vs. device current. Fundamental device linearity studies have shown theoretically that the Ft curve vs. device collector current density (Jc) has an important role in minimizing the intermodulation distortion.[9-12] As early as 1974, Poon [9] demonstrated theoretically that the third-order device distortion in a common-emitter configuration is determined by the degree of non-linearity of the Ft vs. Ic curve, i.e. the more linear the Ft curve, the smaller the IM3. He also demonstrated that a more linearized Ft curve can be achieved by grading the collector.

One direct observation from Poon's work is that the same can be achieved by avoiding the base pushout (Kirk effect) for the entire current operation range. On the same topic, Iwamoto [10] used three different epitaxial structures with various uniform collector doping levels and thus different base pushout onset (onset of the Kirk effect versus current density) to demonstrate experimentally that the curvature in the Ft curve is related to the value of the IP3 (third order intercept). Smaller curvature of Ft results in higher IP3 (lower IM3), with a minimum of IP3 occurring at the critical current density for the Kirk effect, J_{crit}. Based on his observations, we can conclude that pushing the J_{crit} beyond the operating current while maintaining a low variation in Ft will result in increased device linearity.

Furthermore, Iwamoto [11] showed theoretically that harmonic and intermodulation parameters are sensitive to different order derivatives of the Ft versus Jc curve, specifically second-order distortion is related to the first derivative of the Ft vs Jc [Eq. 1], while third-order distortion is related to both the slope and the curvature (first derivative and second derivative) of the Ft vs Jc curve.[Eq. 2]

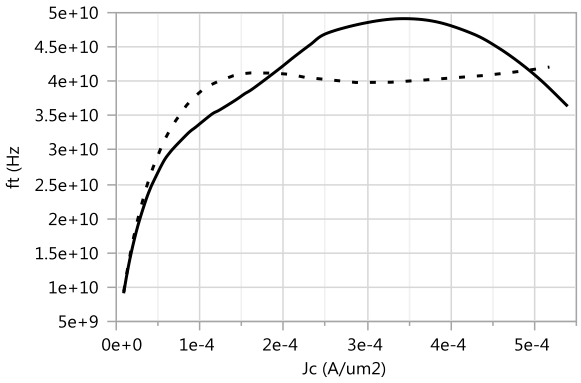
Normally for HBTs, Ft peaks at Jcrit, as shown in Figure 3, the curves with solid line. Based on previous theoretical studies, the third-order distortion is more difficult to minimize since it is influenced by both the slope and curvature of this curve. At Jcrit, the slope is zero but the

curvature is at a maximum. Moving away from Jcrit, the curvature is minimized but the slope becomes significant. Ideally the third-order distortion can be minimized only if the Ft curve is flat.

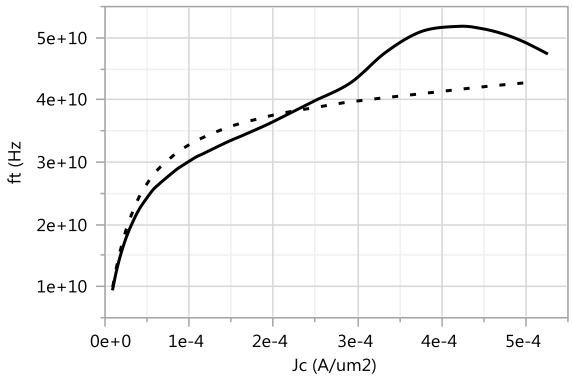
$$\frac{1}{IP_2} \sim \left(\frac{1}{F_t}\frac{\partial F_t}{\partial J_c}\right)^2 \quad \textbf{(Eq. 1)}$$

$$\frac{1}{IP_3} \sim \left(\frac{1}{F_t}\frac{\partial F_t}{\partial J_c}\right)^2 + \frac{1}{2F_t}\frac{\partial^2 F_t}{\partial {J_c}^2} \quad \textbf{(Eq. 2)}$$

Figure 3 shows the comparison between our new epitaxial device and our standard material. The improved structure shows a very flat Ft profile above a current density of about 0.1 mA/μm^2 at low Vce of 0.8V with very little curvature, while higher Vce Ft profiles display no curvature and minimum slope. These Ft curves suggest that the new device should have less intermodulation distortion above 0.1 mA/μm^2.



(a)



(b)

Figure 3. Ft vs Jc curve at (a) Vce=0.8V and (b) Vce=1.5V (dashed line is the improved structure).

Today's new modulation schemes become more complicated with high peak to average power ratio, such as WiMAX and LTE. The introduction of envelope tracking to increase the amplifier overall efficiency also demands high device peak PAE, with the device operating in compression. Under these conditions, the device will see strong non-linearities due to the large signal swing. For this reason, the linearity of the Ft curve at high current densities (saturation) and lower voltages becomes important. Figure 4 shows the comparison of the Ft curve versus Vce for a current density of 0.25 mA/μm^2 between the improved epitaxial design and the standard material.

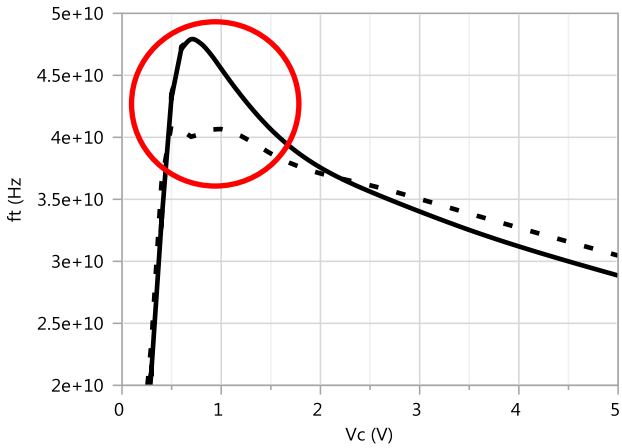


Figure 4. Ft vs. Vce curve at Jc=0.25 mA/μm^2 (dashed line is the improved structure).

The new device shows less variation in Ft over the entire operating voltage and, most importantly, it displays significant less Ft peaking at low Vce, which should improve the device linearity performance closer to saturation.

MEASUREMENTS OF DEVICE LINEARITY

To quantify the device linearity improvements, power measurements were performed on select devices in an on-wafer loadpull environment using a Maury on-wafer loadpull station with mechanical tuners. The devices were first tuned for either maximum power out (Pout) or maximum efficiency (PAE) at a frequency of 1.9 GHz, with no harmonic tuning. For intermodulation measurements a CW signal was used with a tone spacing of 5 MHz. The devices were biased with a base voltage source while using a base ballast resistor and targeting a quiescent current density of approximately 0.01 mA/μm^2.

Figure 5 displays the resulting IM3 measurements for both tuning cases for a sample device of approximately 60 μm^2 over an input power range from -28 dBm to -2 dBm. In this case P1dB occurs at approximately -10 dBm of input power. For the improved device the maximum IM3 is achieved at -7 dBm of Pin which corresponds to a bias current of 6 mA (0.1 mA/μm^2) for the max PAE tune, and at

-12 dBm Pin for the same current density at max Pout tune. In both cases, the maximum IM3 is -10 dBm for the improved device compared to approximately -5 dBm for our standard HBT.

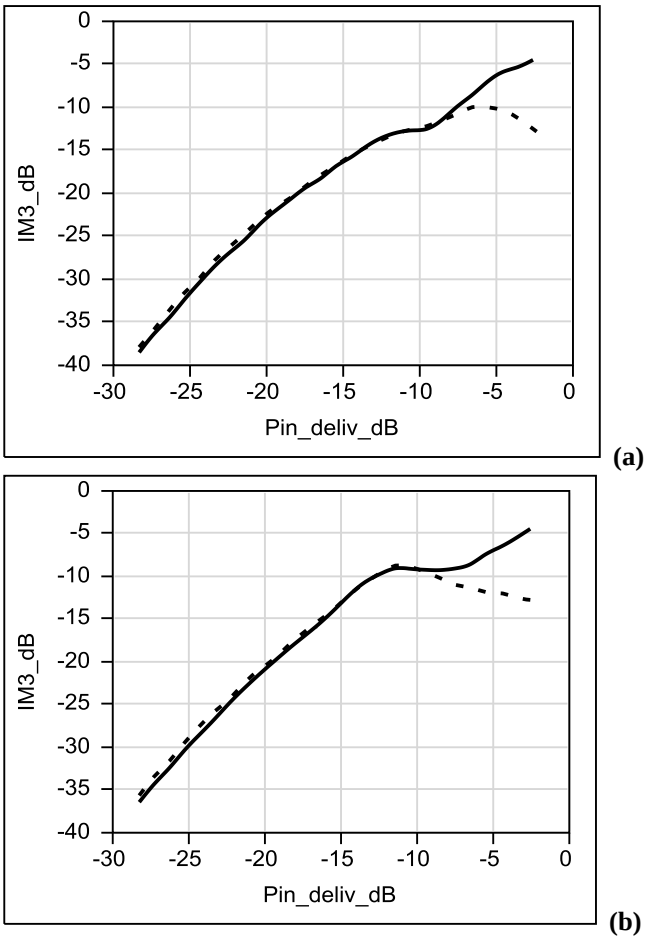


Figure 5. Intermodulation distortion IM3 vs device delivered input power for (a) maximum PAE tuning and (b) maximum Pout tuning.

The resulting intermodulation distortion is significantly improved, especially at higher saturation regime. The very good correlation between the onset of the Ft vs. Jc flatness and the onset of the decreasing IM3 further validates the need for flat Ft vs. Jc epitaxial material for linear applications.

CONCLUSIONS

In conclusion, with this work we report on a novel epi profile with engineered Ft curve, a more flat Ft with current density, which results in improved device linearity. The new epitaxial structure is very well suited for applications where high device linearity is required. To our knowledge, this is the first experimental work to report a flat Ft vs. Jc curve through collector doping profile engineering which results in enhanced device linearity.

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ACRONYMS

HBT: Heterojunction Bipolar Transistor
BiFET: Bipolar / Field Effect Transistor
Ft: Cutoff frequency