Advanced bonding techniques for photonic integrated circuits

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Abstract

The increase of data volume approximately parallels Moore's law, thus leading to a bottleneck in today's networks. While in metro and long haul networks optical communication is well established for many years optics becomes more and more mandatory in short range. To enable optical data transfer for rack to rack or eventually chip to chip applications silicon photonics will be the core technology. Silicon photonics allows combining the benefits of mature Si technology and the superior optical properties of III-V materials. In order to realize such devices, heterogeneous integration of the compound semiconductors on silicon are a key factor. While growth of III-Vs on silicon shows limited success till now, as well as getting the active regions close enough to the silicon waveguides shows to be challenging, wafer bonding overcomes these challenges.

Thus, wafer bonding is the preferred solution as it allows integrating defect free structures with highest performance on the SOI platform. Wafer bonding with optical transparent interfaces is the enabling technology to join III-V materials with silicon in order to realize optical data transfer on a single chip even in high volume production.

INTRODUCTION

Most of today's applications rely on silicon. However, silicon has its limits. Especially when it comes to optoelectronics or high frequency applications, silicon has inherent material restrictions. Researchers came up with great new materials and device combinations. Major obstacles remain, though, how to facilitate this technology on low enough cost to everybody. Here, silicon technology, again, plays a major role, where yields are high and manufacturing is greatly optimized. One solution is to enable functions already at a substrate level by material engineering. These so-called engineered substrates enable new functionality and heterogeneous integration by novel materials or the combination of different materials for optimized device performance. Fusion of different functionalities on one chip is a central topic of engineered substrates.

Wafer to wafer or chip to wafer bonding of compound semiconductors allows the implementation of high performance devices on a low cost silicon platform. This gained a lot of interest in versatile fields as electronics, optoelectronics, spintronics, biosensing, and photovoltaics.

Focusing on photonic integrated circuits (PICs), which are based on SOI fabrication infrastructure, heterogeneous integration of III-V materials, such as indium phosphide (InP), enables high performance devices at low cost and high volumes. The SOI platform is compatible with CMOS technology and hence is highly accurate and mature, leading to a robust, high-yield and reproducible technology and hence performance. Heterogeneous integration gives this platform access to high-speed and efficient III/V-based photonic components [1].

In this way the hybrid silicon platform heterogeneously integrates III/V functionality on the SOI platform by means of molecular wafer bonding. In particular fusion wafer bonding has been proven to enable sufficient bonding without degrading optical performance of the III-V materials and efficient optical coupling to the SOI waveguides.

FUSION WAFER BONDING

Direct wafer bonding is a technology to join two substrate materials with different structural properties. Additionally, plasma activation of both wafer surfaces can be used to change the surface chemistry of both materials and therefore reducing the bonding temperature. In this way, materials supporting a high crystal quality of compound semiconductors can be joined with a carrier that accounts for differences in thermal expansion. In this way, it is possible to have Si-based waveguides and modulators next to III-V laser diodes.

Direct wafer bonding has many advantages in comparison to direct growth of III-Vs on silicon. In many cases fusion wafer bonding uses Silicon dioxide (SiO_2) films on both wafers for the bonding process. The oxide films can be patterned or blanket. Fusion bonding requires flat wafers with a surface roughness of less than 1nm, which is well within the capabilities of today's CMP equipment. SiO_2 is a known CMOS-compatible material, and oxide deposition and CMP can be performed on practically all wafers. The resulting bond interface does not imply any limitations to further downstream processing, i.e., further processing steps

can happen in a high vacuum or at temperatures higher than the bonding temperature itself.

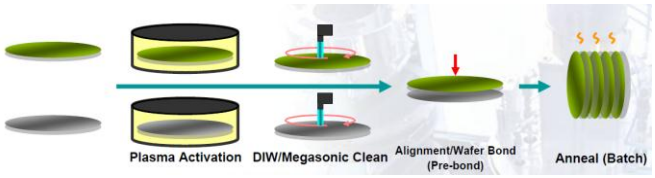

Figure 1: Fusion wafer bonding process flow

Fusion wafer bonding is a two-step process consisting of a room temperature pre-bond and an annealing step. Traditional annealing processes developed for SOI wafer manufacturing required an annealing temperature of 1100°C. Those thermal annealing temperatures required are far too high for CMOS and III-V technology, in which the main temperature limitation is imposed by the metal temperature limits or interdiffusion (400°C or 450°C for very short time, in the range of minutes). The development of plasma activation of the wafer surfaces was the technical break-through which enabled the widespread use of fusion bonding for CMOS and III-V devices.

PLASMA ACTIVATION

Low temperature plasma activated direct wafer bonding is a process that lowers the required annealing temperatures necessary for reaching high bond strength. One example for such an improvement is a pair of native oxide - thermal oxide wafers, where bulk strength can be achieved by plasma activation of wafers prior to bonding with subsequent annealing at 300°C for a short time (0.5 - 1 hour). Figure 2 shows the surface energy (bond strength) characteristics as a function of the annealing temperature for Si/SiO_2 wafer pairs with and without plasma activation prior to fusion bonding. This is shown in more detail by Plach et al. [2].

This makes fusion wafer bonding compatible with fully processed CMOS wafers. This fusion bonding process can be easily adopted for compound semiconductors with a pre deposited SiO_2 layer on top. Fusion wafer bonding has several advantages compared to other bonding techniques, which makes it particularly suitable for PICs. Pre-bonding happens at room temperature and therefore there is no thermal expansion of the wafers and the SiO_2 interface is compatible with the required optics. The pre-bonding process itself is very fast, which allows throughput of currently up to 15 wafers per hour per wafer bonding system. After pre-bonding the wafer stack can be inspected for bond defects and alignment accuracy. In case any parameter is outside of specification then the 2 wafers are just separated, cleaned and bonded again. There is no other wafer bonding technique that allows such an easy rework routine.

Finally as annealing is performed as batch process the total cost-of-ownership (TCO) of fusion bonding is significantly better than other bonding methods [3].

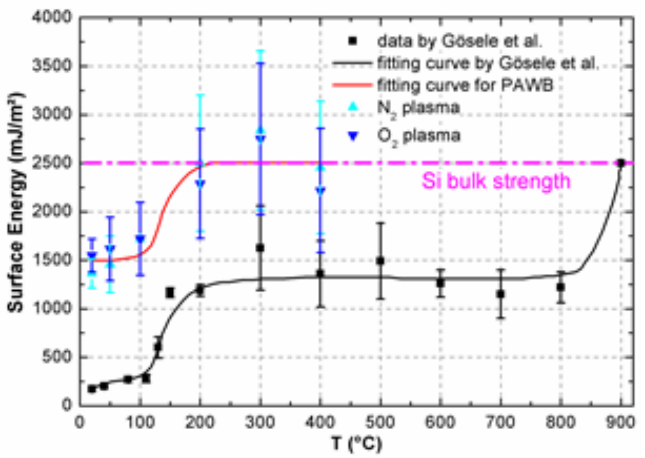

Figure 2: Surface energy of bonded Si/SiO2 wafer pairs annealed at various temperatures for high temperature oxide bonding and plasma activated wafer bonding using N2 respectively O2 plasma. The maximum bond strength of 2.5J/m² is indicated by the dashed-dotted horizontal line. Data for high temperature process was taken from Ref. [4].

Figure 3 clearly shows that high surface energy and therefore good bond strength is achieved by oxygen plasma activation. The optimization of this process is investigated for different annealing temperatures. Furthermore it is demonstrated that lower annealing temperatures can be offset by extending annealing duration. Thus plasma activation is enabling heterogeneous integration of different materials with diverging thermal expansion coefficients, e.g., indium phosphide (InP)-on-Si or gallium arsenide (GaAs)-on-Si by implementation of a thin SiO_2 interlayer.

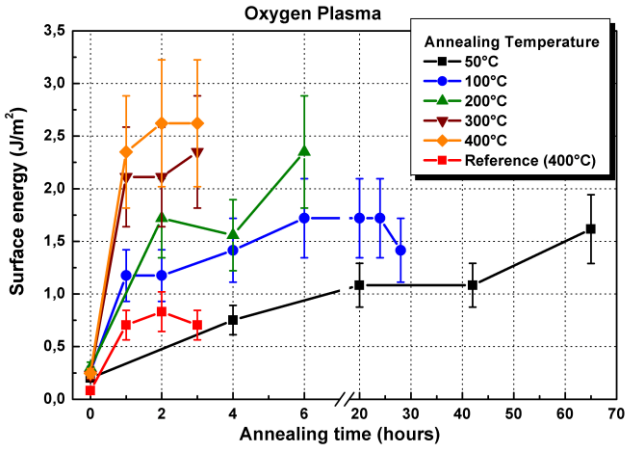

Figure 3: LowTemp™ plasma activation with oxygen plasma enables high bond strength at moderate annealing temperatures.

ADVANCED CHIP TO WAFER BONDING

As many designs of PICs only require heterogeneous integration on a minor part of the SOI wafer costs can be significantly reduced by a chip to wafer approach. Costs can even be reduced further by applying advanced chip to wafer (AC2W) bonding techniques with a wafer level approach. This is especially the case as in contrast to wafer to wafer fusion bonding for chip to wafer heterogeneous integration additionally to plasma activation still bond force and elevated temperatures are needed to gain sufficient bond strength and high yield.
The AC2W bonding process is a process flow for chip to wafer bonding especially designed for application of force

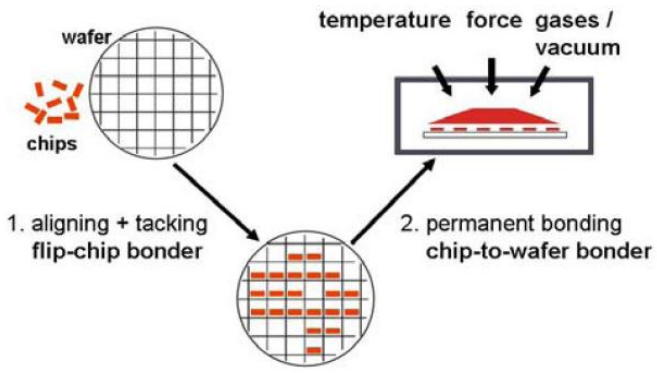

Figure 4: The AC2W process flow

and temperature while forming the bond at a throughput appropriate for volume production. The concept of separation of aligning substrates and then bonding the substrates to each other is well known and widely used for wafer to wafer bonding. At the AC2W bonding process the same concept is adapted to chip to wafer bonding.
The AC2W process is a two-step process as depicted in Figure 3. First all chips are aligned and tacked to the wafer, second all chips are bonded in parallel simultaneously permanently to the wafer [5].
The permanent bonding process requires a controlled, homogeneous force to be applied on every single chip. To accomplish this, the pressure plate is equipped with a flexible, compliant layer that compensates for any thickness variations between the top chips when applying the bond force via the piston and the pressure plate.
As depicted in figure 4, the compliant layer compensates for possible pressure non-uniformities caused by die or target wafer variations. Thickness variations of the dies are an important point to be addressed as they occur regularly when the dies originate from different source wafers. The variations are usually in the range of tens of micrometers or below. With the compliant layer yield issues caused by die to die or target wafer variations can be significantly reduced.

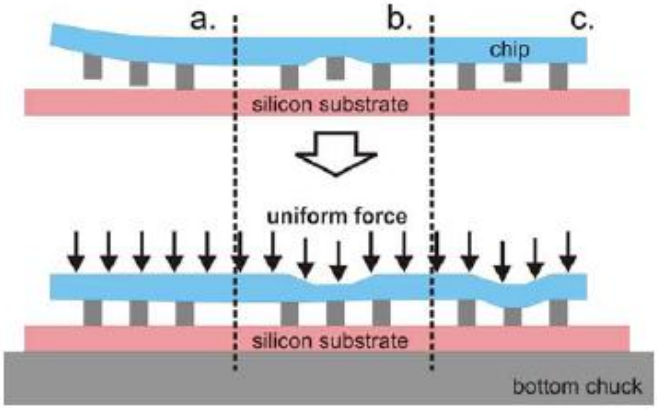

Figure 5: Unbonded areas can occur if not compensated e.g. by a. bow or warpage, b. unevenness of the substrates, c. height variation of the dies (top). These issues can be overcome by uniform application of force on the backside of the die by the usage of a compliant layer

COST OF OWNERSHIP

Wafer to wafer (W2W) bonding is a widely used process approach for connecting and stacking devices on. The main advantage of the W2W bonding is the very high achievable alignment accuracy in the sub-micrometer range with high throughput.
At flip chip bonders the throughput depends strongly on the targeted alignment accuracy. Therefore the throughput at the first step of the AC2W drops when accuracies below 2 micrometer are targeted while at W2W it stays nearly constant for all. At the second step of the AC2W the high throughput of W2W bonding is also achieved since it is very comparable to W2W bonding as there are also multiple dies bonded to the target wafer at once. Also the process time and process recipe is quite the same.

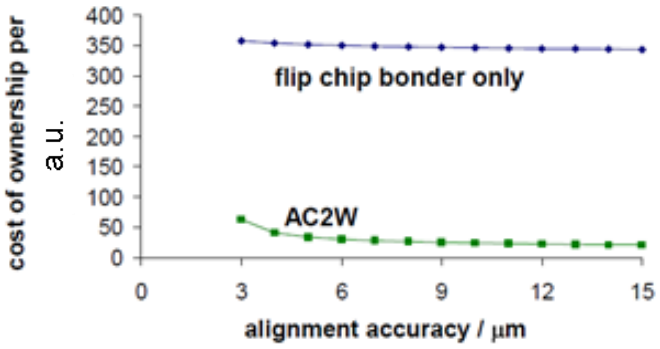

Figure 5: Cost of Ownership comparison of Flip chip bonder only and AC2W bonding proces.

For better understanding here an example will be given. It is assumed that 2641 chips with a size of 5 x 5 mm² are bonded to a 300 mm wafer.

An interconnection time of 20s for bonding is assumed and additional alignment time on a flip chip is about 0.5s. It has to be mentioned that for heterogeneous integration the bonding time can be significantly longer. This means that at the flip chip bonder only process each individual die needs (20s + 0.5s =) 20.5s to be bonded to the wafer which results in a throughput of about 175 dies per hour or 0.066 wafer per hour.

At the AC2W process the throughput of the two steps has to be evaluated separately. At the first AC2W step the throughput is determined by the flip chip bonder alignment time (0.5s) and therefore about 7200 dies per hour or 2.73 wafers per hour. Besides the throughput there are several variables that affect the cost of ownership of the AC2W process, as the die size, wafer size, bond process and alignment accuracy. For the given example the cost of ownership (CoO) was calculated and it shows a cost advantage of one order of magnitude as shown in Figure 5.

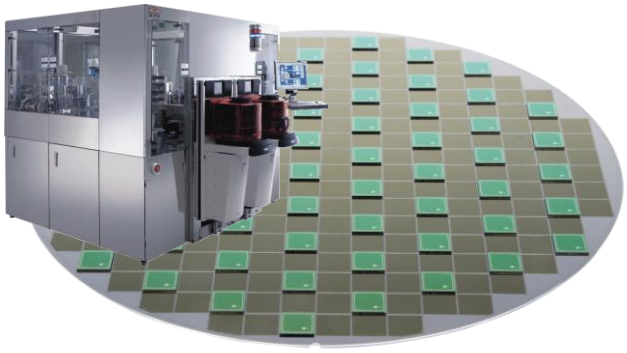

Figure 6: Advanced Chip to wafer bonded dies on a 200mm wafer.

SUMMARY

Heterogeneous integration for silicon photonics has caught a lot of attention recently. Despite the concentrated efforts to directly grow III-Vs onto silicon, dislocations are hard to control. Wafer bonding offers an ideal solution for this problem. Direct wafer bonding process enables high quality compound semiconductor films to be transferred on any substrate. In this way, different semiconductor layers can be stacked, enable to have different functionalities on one single wafer. Advanced bonding techniques for photonic integrated circuits or heterogeneous integration in general can add tremendous benefit for device fabrication and production costs. In particular, plasma activation for wafer fusion bonding enables low temperature processes thus avoiding high bonding temperatures and reducing thermal stress or outgassing issues.

Wafer level chip to wafer bonding as shown with the AC2W process are a significant progress for cost of ownership models. Compared to other approaches like flip chip bonder only or wafer to wafer bonding it offers less material consumption at high yield and throughput and therefore is best suited for high volume chip to wafer production.

ACKNOWLEDGEMENT

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