AlGaN/GaN MOS-HEMTs using RF Magnetron Sputtered SiO_2 Gate Insulator and Post-Annealing Treatment

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Abstract

We propose high-quality RF magnetron sputtered SiO_2 gate insulator for high-voltage AlGaN/GaN MOS-HEMTs. A very high dielectric breakdown field over 9.6 MV/cm of SiO_2 insulator was achieved by adding oxygen flow during sputtering process. A post-annealing treatment was further developed to recover the sputtering-induced surface damage. After post-annealing, carrier concentration and mobility in 2DEG channel were improved by 21.7 and 5.5 %, respectively. As a result of optimized sputtering and post-annealing conditions, we achieved a very high breakdown voltage of 205 V at relatively short gate-drain distance of 2 μm (breakdown field of 102.5 V/μm).

INTRODUCTION

Although AlGaN/GaN HEMTs have attracted considerable attention for high-power, high-speed, and high-temperature applications, a relatively large leakage current through Schottky-gate contact and the surface traps remain as a serious problem [1]. In order to improve reverse blocking characteristics, significant progress has been made on MOS-HEMTs using various insulating materials.

A SiO_2/AlGaN/GaN MOS-HEMT is a suitable structure for suppression of leakage current and increase of breakdown voltage due to the wide bandgap of SiO_2 and the high conduction band offset at SiO_2/GaN interface [2]. However, further investigation into SiO_2 gate insulator is required to increase breakdown voltage and V_{GS} sweeping range. Various deposition techniques, such as PECVD, E-beam evaporation, and ALD, have been reported for deposition of SiO_2 on GaN devices [3-5].

In this paper, we propose RF magnetron sputtered SiO_2 and optimize its deposition and post-treatment conditions for high-voltage AlGaN/GaN MOS-HEMTs. RF magnetron sputtering has proved to be capable of depositing SiO_2 on GaN with quality better than the above-mentioned techniques [6], the reason being that energetic particle impingement can make the growing film more condense thus enhancing the oxide breakdown field. However, due to the difficulty in preventing the bombardment damage to the GaN epilayer that degrades the 2DEG properties, there are very few reports on the successful fabrication of AlGaN/GaN MOS-HEMTs employing sputtered SiO_2 gate insulator.

OPTIMIZATION OF SiO_2-SPUTTERING CONDITIONS

Al/SiO_2/n^+-GaN (n = 1.4 × 10^{19} cm^{-3}) MOS-capacitors were fabricated to examine breakdown field of the SiO_2 film under different deposition conditions. The sputtering was carried out at room temperature with a constant power of 160 W. Argon/oxygen gas mixtures were used as the sputtering gas with the ratio from 0 to 40 % to find optimum condition for high breakdown field. The breakdown voltage of the SiO_2 film strongly depends on oxygen flow rate as shown in Fig. 1. The breakdown voltage was improved with increase of oxygen ratio up to 30 % to achieve the highest value of 9.6 MV/cm. The oxygen flow introduces oxygen atoms into the film and densifies SiO_2 insulator. Beyond 30 % oxygen ratio, breakdown voltage started to decrease, which is attributed to the reduction of energy input into the film due to the smaller atomic mass of O than Ar, reducing the film density. The sheet carrier concentration and the electron mobility in SiO_2/AlGaN/GaN sample using 30 % oxygen condition were decreased by 25 and 69 % due to sputtering damage to AlGaN surface. These damages were recovered after post-annealing treatment as shown in Table 1. It is seen that the post-annealing at 900 ˚C for 20 s is able to fully restore the epilayer crystallinity and interface quality. The largest breakdown field of 9.6 MV/cm is higher than that of the SiO_2 films deposited on GaN by any other techniques including PECVD, photo-CVD, and E-beam evaporation [7-9].

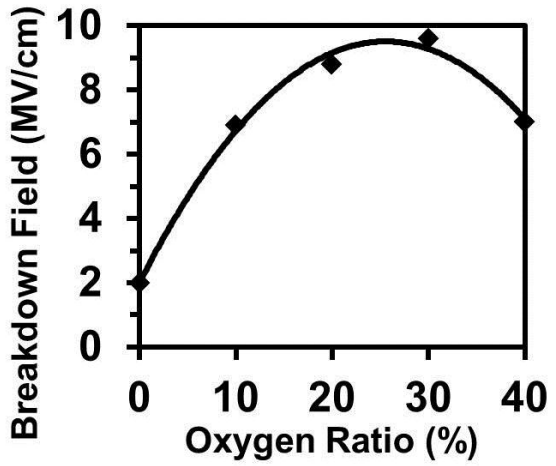

Fig. 1: Breakdown field of the sputtered-SiO_2 films on n^+-GaN as a function of oxygen ratio in the sputtering gas.

Table 1: Values of the electron concentration (n_s) and mobility (μ) under different annealing temperatures and durations.

Experimental conditions	Electron mobility ($cm^2/V \cdot S$)	Sheet concentration ($\times 10^{13}$ cm^{-2})
Epilayer	1060	1.08
RTA (0 ˚C, 0 s)	330	0.81
RTA (800 ˚C, 20 s)	644	0.98
RTA (900 ˚C, 20 s)	1118	1.32
RTA (1000 ˚C, 20 s)	1077	1.30
RTA (900 ˚C, 10 s)	941	0.99
RTA (900 ˚C, 30 s)	1116	1.31
RTA (900 ˚C, 60 s)	974	1.25

ALGAN/GaN MOS-HEMTS USING RF-SPUTTERED SiO_2 GATE INSULATOR

Cross-sectional view of the fabricated SiO_2/AlGaN/GaN MOS-HEMT is shown in Fig. 2. 220 nm-deep mesa isolation and 40 nm-deep recessed source/drain etching were carried out by using Cl_2-based ICP-RIE. Next, 10-nm SiO_2 was sputtered at room temperature with O_2/Ar ratio of 30 %, which is the optimized condition, and showed the highest dielectric breakdown field. Ti/Al/Ti/Au were then deposited by E-beam evaporation as the Ohmic contacts, followed by post-annealing in N_2 ambience. Deposition of gate metals (Ni/Au) completed the fabrication process. As for the device dimensions, the gate length, width, source-to-drain, and gate-to-drain distances were 2, 100, 6, and 2 μm, respectively.

Table 1 shows the values of n_s and μ under different annealing temperatures or durations. It is seen that the post-annealing at 900 ˚C for 20 s is able to fully recover the sputtering-induced surface damage to epilayer. The additional improvement in both n_s (21.7%) and μ (5.5%) is due to the chemical passivation of the exposed epilayer surface dangling bonds by the SiO_2 film. Further increase in the annealing temperature or time resulted in reduction of n_s and μ again, owing to the defect generation by AlGaN/GaN film dissociation at the elevated temperature, which degraded the epilayer crystallinity and channel interface morphology. Furthermore, it was found that the optimized post-annealing condition coincides with that of the GaN-based Ohmic metal annealing for Ti/Al contact scheme, which is generally performed at 850~900 ˚C for 20~30 s. Therefore, the two annealing steps can be combined into one to save the thermal cost and simplify the fabrication process. As a result, our process may be considered to have the lowest thermal energy requirement to realize MOS-HEMTs among all the dielectric deposition techniques, which is certainly beneficial for commercial applications.

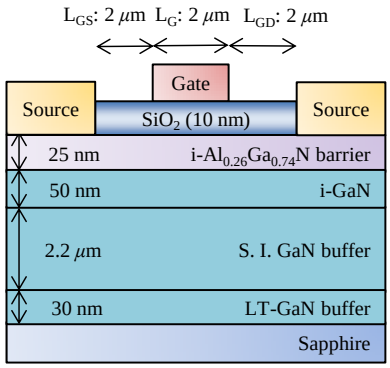

Fig. 2: Cross-sectional view of the fabricated SiO_2/AlGaN/GaN MOS-HEMT.

Output *I-V* and transfer curve of the SiO_2/AlGaN/GaN MOS-HEMT using the optimized annealing temperature of 900 ^oC are shown in Fig. 3. For the characterization, the gate leakage current of the MOS-HEMT was first compared with that of the conventional HEMT of the same dimensions. It was found that at a reversed gate bias of −30 V, more than four orders of magnitude lower leakage current was achieved by using the MOS-HEMT. The peak drain current and the maximum transconductance were 594 mA/mm and 74.5 mS/mm, respectively. The three-terminal off-state breakdown voltage was measured by a curve tracer and was 205 V. A comprehensive comparison of the breakdown voltages per unit gate-drain distance, obtained from various publications [8-15], is presented in Fig. 4. The dielectric thickness is also taken into consideration since a direct comparison using MOS-HEMTs with the same dielectric thickness is difficult. The breakdown voltage performance of our device is, if not better, at

least on-par with other GaN-based MOS-HEMTs reported to date.

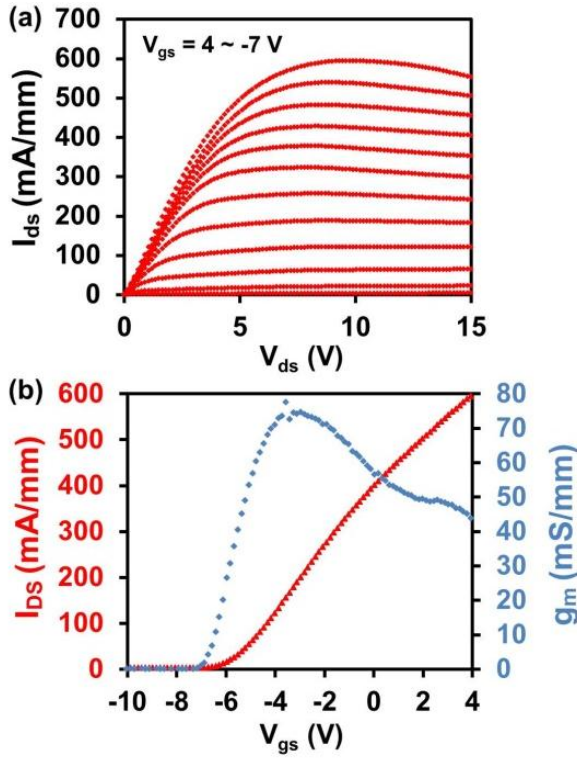

Fig. 3: (a) Output *I-V* and (b) transfer characteristics of the SiO_2/AlGaN/GaN MOS-HEMT with 10-nm-thick sputtered-SiO_2.

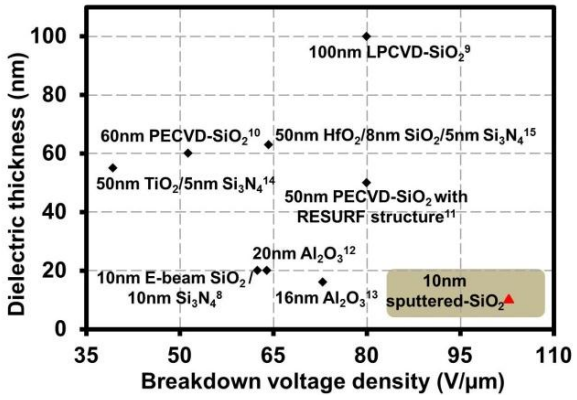

Fig. 4: Comparison of breakdown voltage density of MOS-HEMTs achieved by different groups.

CONCLUSIONS

Using room-temperature RF magnetron sputtering with a 30% oxygen mixing, highly condensed SiO_2 has been demonstrated to be a suitable gate insulator for AlGaN/GaN MOS-HEMTs. In addition, post-annealing treatment during Ohmic contact formation removed the sputtering-induced damage to GaN epilayer, resulting in a MOS-HEMT with high saturation current and off-state breakdown voltage.

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ACRONYMS

HEMT: high electron mobility transistor
MOS: metal-oxide-semiconductor
2DEG: 2-dimensional electron gas
PECVD: plasma-enhanced chemical vapor deposition
ALD: atomic layer deposition
n_s: electron concentration
μ: electron mobility
RTA: rapid thermal annealing