# A Simulation of Wafer Temperature-Time Profile in PVD Process Using an Exponential Model and Its Applications

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**Abstract**

**The wafer temperature-time profile is very important for semiconductor processes, especially for PVD deposition. In this paper, a wafer temperature-time simulation method is developed using an exponential function to model the PVD process. This simulation can give semi-quantitatively the wafer temperature at a given time at the different stages in a given PVD process. The determination of the parameters for the model is discussed. This simulation can be used to optimize process, compare different PVD processes and for the cycle time reduction.**

## INTRODUCTION

Wafer temperature is a very important factor for Physical Vapor Deposition (PVD) process, because it impacts not only the substrate surface condition, film deposition rate, and file thickness, but also the grain size and orientation [1]. However, knowing the wafer temperature is not easy and measuring the wafer temperature is always a challenging task [2], [3].

Figure 1 shows a simplified diagram of a PVD deposition chamber illustrating the major components which will impact the wafer temperature. In this example the wafer is not clamped throughout the process sequence and no backside gas is applied. Heat is exchanged with a temperature-controlled pedestal or platen and with the chamber by conduction and radiation. It is also receives heat from condensation of deposited material, plasma and reflected neutrals bombardment. The chamber wall or shielding is a large heat sink, which absorbs the heat from the wafer, the amount depending on their temperature difference. Degas, pre-heating, or cooling chamber are very similar to the deposition chamber, except that there is no target or sputtered metal atoms and gas is introduced to aid thermal conduction between the wafer and platen. The wafer itself radiates heat to the environment during the cooling. During the wafer transfer between process chambers, the wafer cools down on a robot arm. For a multiple metal layer PVD deposition process, wafers will go through different heating and cooling processes and it is very difficult to get the real wafer temperature profile during the processes.

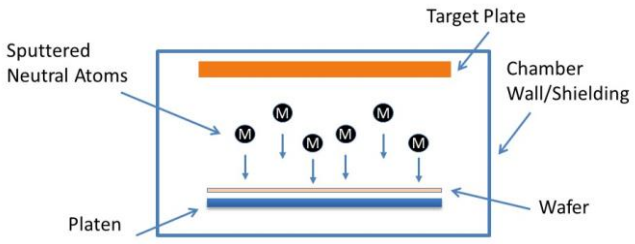



FIGURE 1. A DIAGRAM TO ILLUSTRATE THE HEATING OR COOLING COMPONENTS IN A PVD DEPOSITION CHAMBER.

In this paper, we use an exponential model [4] to simulate the wafer temperature during different PVD processes. The parameter extraction for the model is discussed. An example of using the model for cycle time reduction is given at the end of the paper. The experimental data are extracted from Ref. 2 and 5, in which a Sigma Sputtering System from SPTS Technologies was used. Since the temperature at the wafer edge is different from that at the wafer center, we used the data from the wafer center only for the simplicity. However, the model and the conclusions in this paper can be applied to the wafer edge and over a range of the wafer sizes.

## THEORETICAL MODEL

Figure 2 shows a typical wafer temperature profile during the heating in a PVD module without deposition. The curve can be simulated with an exponential model [4], which can be described through the equation 1 and 2 for the heating and cooling respectively.

$$T = T_i + (T_f - T_i) * (1 - e^{-t/\tau}) \quad (1)$$

and

$$T = T_f + (T_i - T_f) * e^{-t/\tau}, \quad (2)$$

where τ=R*C. R is the system thermal resistance and C is the system heat capacity, dominated by the wafer, but including contributions from the platen, wall or shielding, and the plasma. The wafer is only a part of the system. Therefore, for the different processes, the R, C, and τ will be different and the τ can be obtained from the model by fitting to the experiment data. $T_i$ is the initial temperature of the process, which can be either the room temperature or the temperature reached in the previous step. $T_f$ can be either the room temperature when the cooling or the final equilibrium temperature in the heating. The wafer approaches its equilibrium temperature asymptotically. Due to losses it will rest below the platen set point during heating without plasma. The final temperature can be also extracted by fitting to the experimental data.

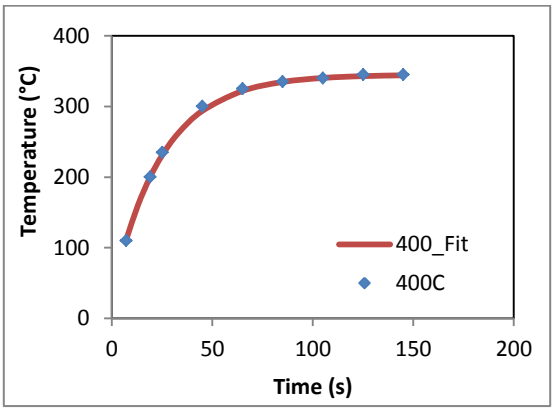



FIGURE 2. DEGAS HEATING WITH NOMINAL TEMPERATURE AT 400°C. THE TIME CONSTANT IS 25S AND $T_F$ IS 345°C IN THE FITTING MODEL.

The diamonds in the Figure 2 are experimental data derived from the degas heating at 400°C nominal temperature setting [2]. The line is the model fitting with a time constant, τ, of 25s. It is a reasonable approximation, over the temperature range of interest, that τ will not change with the temperature setting as long as the chamber pressure and gas flow are kept the same. The final equilibrium temperature here, $T_f$, is 345°C for the model, although the nominal temperature setting is 400°C. Figure 3 shows a correlation of the nominal temperature with the final equilibrium temperature. It can be used for the temperature scaling of the model. With the τ used for the fitting in the Figure 2 and the $T_f$ from Figure 3, we can find the wafer temperature at any time during the degas process with different temperature setting.

Wafers placed on a platen inside the deposition chamber prior to the plasma deposition can be either heating up or cooling down depending on both the platen temperature and the wafer temperature from previous process, which can be degas, Pre Sputter Etch (PSE), cooling, or another deposition. Usually it is very difficult to measure the wafer temperature during a cooling process. The beauty of the model is that we can get the τ from a heating process and use the same τ to determine the wafer temperature during the cooling in the same system, see Figure 4.

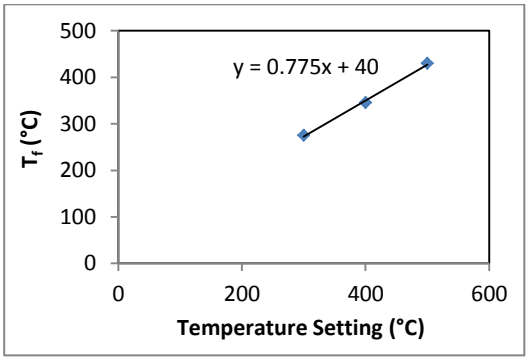



FIGURE 3. THE CORRELATION BETWEEN THE FINAL EQUILIBRIUM TEMPERATURE $T_F$ AND THE NOMINAL TEMPERATURE SETTING.

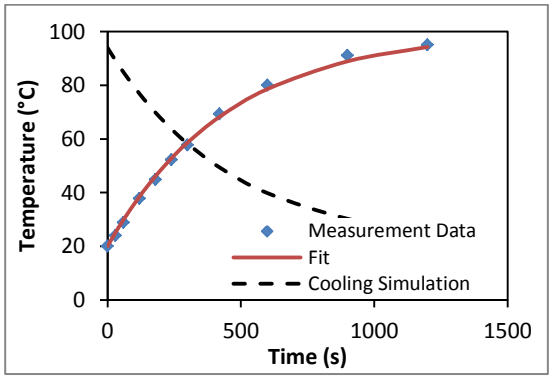



FIGURE 4. PLATEN HEATING AND COOLING SIMULATION WITH THE SAME TIME CONSTANT OBTAINED FROM MEASUREMENT DATA FITTING DURING A HEATING PROCESS.

Wafer heating during deposition is a complex process with plasma energy (target power), gas pressure, gas flow and platen temperature set-point all influencing wafer temperature to varying degrees. Both the plasma power and the platen temperature will heat the wafer. Figure 5a shows the wafer heating curves at 8KW and 12KW separately with the platen temperature setting at 300°C. There are also two fitting curves for 8KW and 12KW respectively. The time constant of each fit can be determined separately. Since the product of the power and the time gives the heating energy, that drives the temperature, we can plot the wafer temperature against the product of the power and the time (power*time) as shown in Figure 5b. Both 8KW and 12KW

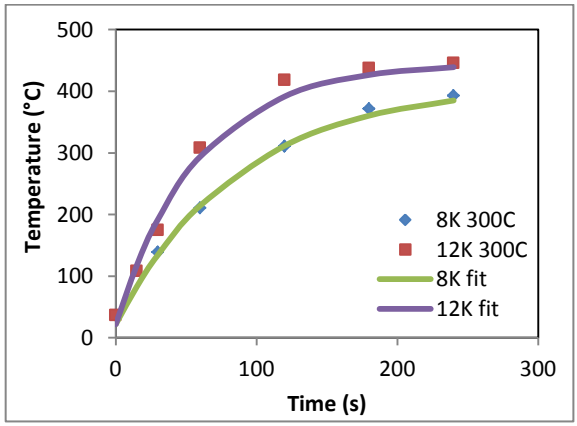
data match each other relative well in the temperature and Power*Time plot and a common time constant ($\tau_{p*t}$) can be extracted from the model by fitting the experimental data to equation 3 below, which is very similar to equation 1.

$$T = T_i + (T_f - T_i) * (1 - e^{-t/\tau_{p*t}}) \quad (3)$$

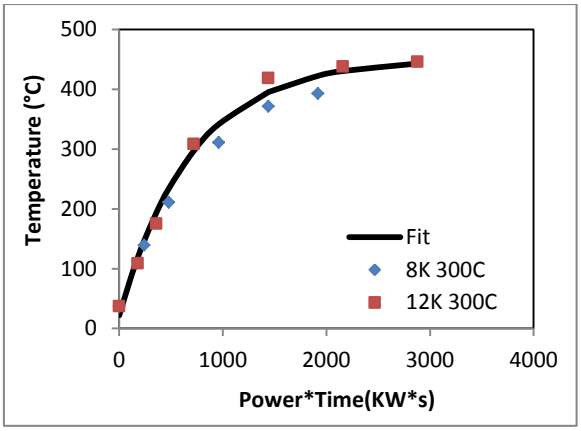
This common power*time time constant ($\tau_{p*t}$) is actually equivalent to the time constant of the unit power (1KW). From $\tau_{p*t}$, the time constant $\tau_p$ for each power condition can be obtained with a simple scaling with equation 4.

$$\tau_p = \tau_{p*t} / Power \quad (4)$$

The time constant $\tau_{p*t}$ used in the fit of Figure 5b is 700s, which gives $\tau_p$ =87.5s for 8KW and 58.5s for 12KW which are used in Figure 5a.



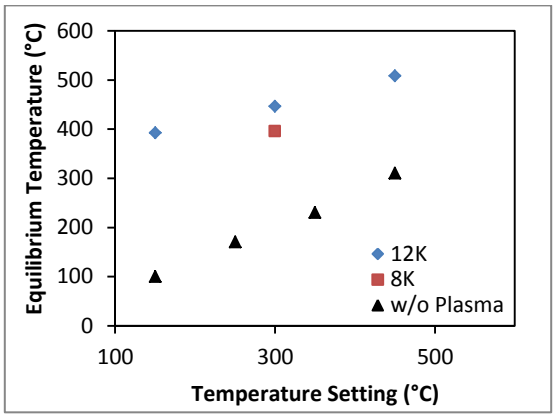

(a)



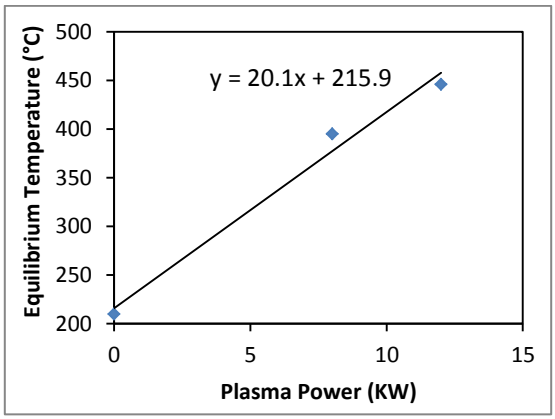

(b)

FIGURE 5. THE WAFER HEATING DURING PLASMA DEPOSITION. (A) 8KW AND 12KW DATA WITH THE EXPONENTIAL MODEL FITTING. THE TIME CONSTANTS USED FOR THE FITTING ARE CALCULATED FROM THE CHART IN (B). (B) POWER*TIME CURVE FITTING FOR THE EXTRACTION OF THE TIME CONSTANT OF THE UNIT POWER (1KW).

Figure 6a gives the relationship of the wafer equilibrium temperature and the platen temperature setting at different plasma power conditions: no plasma, 8KW, and 12KW. A linear correlation between the equilibrium temperature and the platen temperature stetting for each plasma power is observed. To get the scaling parameter of the equilibrium temperature at the different plasma power and different platen temperature settings, a correlation of the equilibrium temperature versus the plasma power at the 300°C of the platen temperature setting is shown in Figure 6b. The equilibrium temperature of the "no plasma" condition at 300°C is estimated from the linear correlation in Figure 6a. Based on Figure 6b, the correlation of the equilibrium temperature and the plasma power may also be assumed to be linearly related. Therefore, the data in Figure 6a allows us to extrapolate all the equilibrium temperatures at various plasma powers and platen temperatures.




(a)




(b)

FIGURE 6. THE EQUILIBRIUM TEMPERATURE AS FUNCTIONS OF (A) THE PLATEN TEMPERATURE SETTING AND (B) THE PLASMA POWER.

## APPLICATIONS

This simulation of the wafer temperature-time profile in PVD processes using the exponential model has many applications. One of them is the cycle time reduction. The example here is the evaluation of the degas time. Figure 7 shows the simulated wafer temperature as a function of the degas time at different platen temperature settings. Assume

that a wafer temperature of 300°C is required for the effective degas, it needs 85s to reach 300°C for a 350°C platen temperature setting, 47s for 400°C setting, and only 36s for a 450°C setting. Therefore, we can get a 50%+ degas time reduction by increasing the nominal platen temperature setting without varying the real wafer temperature based on the simulation here.

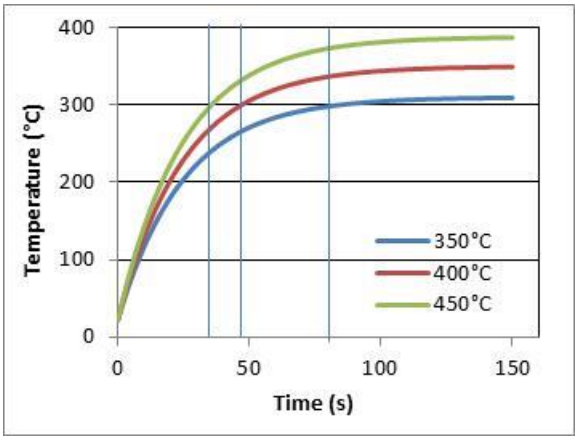



FIGURE 7. THE WAFER TEMPERATURE SIMULATION OF THE DEGAS PROCESS AT DIFFERENT PLATEN TEMPERATURE SETTING.

## CONCLUSIONS

We used an exponential function model to simulate the wafer heating or cooling in SPTS PVD sputter system. This simulation can be used semi-quantitatively to describe the wafer temperature as a function of the time, the plasma power, and the platen temperature. It can be used in many applications, such as the cycle time reduction and the process evaluation.

## ACKNOWLEDGMENTS

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## REFERENCES

[1] K. H. Guenther, *Revisiting structure zone models for thin film growth*, Modeling of Optical Thin Films II, San Diego, CA, USA, 1990
[2] P. Rich, *Thermal Characterization of the Sigma Sputtering System*, Electrotech Technical Report, Sept. 1993
[3] R. A. Powell, et al, *PVD for Microelectronics: Sputter Deposition Applied to Semiconductor Manufacturing*, 1999
[4] http://en.wikipedia.org/wiki/Time_constant#Thermal_time_constant
[5] SPTS Data Sheets

## ACRONYMS

PVD: Physical Vapor Deposition

PSE: Pre Sputter Etch