Analysis and Optimization of a Through Substrate Via Etch Process for Silicon Carbide Substrates

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Abstract

Through substrates vias (TSVs) are an important design feature to facilitate chip mounting, to enhance electrical performance especially at high frequencies and to yield good heat spreading. To process TSVs in silicon carbide (SiC) as base material, the SiC wafers are bonded by means of a temporary wafer bond process to a supporting carrier, thinned to the desired target thickness, furnished with an etch mask, and then etched by means of a plasma etch process.
We have analyzed the stress in the wafer stack due to the bonding and plasma etch processes. We found that the stress in the wafer-carrier sandwich due to bonding originates mainly from the different coefficients of thermal expansion of the materials. The bow of the wafer-carrier composite during the etch process in the plasma reactor was measured in real time with an *on-line* sensor. The effects of the mechanical mounting of the composite in the reactor and the helium back cooling as well as the impact of the etch plasma could be determined independently. This allowed to develop an etch process that exerts less stress and minimizes mechanical failure of the wafers.

INTRODUCTION

Through substrates vias (TSVs) are an important feature to facilitate chip mounting and to enhance electrical performance at high frequencies by minimizing the inductance.
The high breakdown voltage and the high electron mobility make gallium nitride (GaN) an attractive material for various high performance applications. As GaN is often epitaxially grown on SiC wafers, the processing of TSVs involves the preparation of holes in SiC and GaN. Compared to silicon or gallium arsenide, these materials are much more difficult to etch and require rather harsh etch conditions. FBH has developed and implemented a process flow for the fabrication of TSVs in silicon carbide wafers for GaN-based power bars and MMICs. The TSV backside process is performed after completion of the front side process. The 100 mm wafers are bonded to a 105 mm wafer carrier with HT10.10 as temporary adhesive. The wafers are thinned by lapping and polishing to their desired thickness of 100 µm. The etch mask for the via etch process consists of a 500 nm thick aluminum and a 3000 nm indium tin oxide (ITO) layer. This material combination allows the plasma etching of vias in 100 µm thick SiC with sizes down to 20x80 µm². The etch process is performed in a Sentech SI500 ICP etch chamber with a SF_6/He gas mixture. Then, the remaining mask is stripped in diluted KOH and the GaN-based epitaxial layer is etched in another SI500 ICP tool using Cl_2 plasma. After deposition of a Ti/Au plating base, 5 µm of gold are electroplated. Finally, the wafer is debonded from the carrier, cleaned and diced. The cross section of a typical via obtained with this process is shown in fig 1.

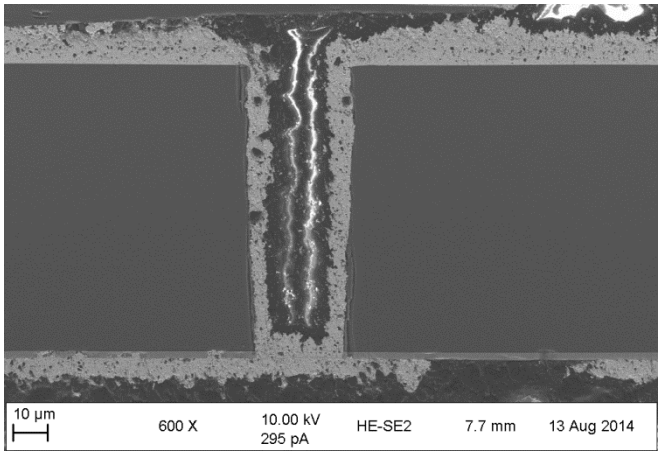

Fig. 1 Cross section of a TSV in 100 mm SiC obtained with FBH's via process.

CHALLENGES

SiC is mechanically very hard and chemically rather inert, which makes plasma etching of TSVs very difficult [1,2,3] even if the wafer is thinned to 100 µm. Etching mask, carrier material, ICP and RF power density, and process temperature strongly affect the result. To sustain a productive etch rate, platen temperature and reaction heat have to be as high as possible without causing delamination of the thinned wafer from its carrier. Due to the low etch rate in the order of 0.5 µm/min, a long term resistant hard mask is required, which in our case is formed by the Al/ITO

layered mask. The carrier material must be transparent to allow for lithographic access of the wafer's front, must provide efficient and uniform heat conduction, and it must have a similar coefficient of thermal expansion to avoid excessive stress when etching SiC at elevated temperatures. The fixture of the wafer-carrier composite has to allow for temperature control by cooling using a helium flow at the back, uniform etching, and minimum mechanical stress on the wafer.
To study the impact of the various parameters on the wafer bow and hence the stress on the system, an independent measurement of their impact on the wafer bow in the etch chamber is required.

EXPRIMENTAL

To access the mechanical distortion of the system wafer-carrier in the plasma etch chamber during etching, a commercially available wafer bow metrology system (EpiCurve®, LayTec AG) was used. This system was originally developed for controlling the epitaxial growth in high temperature MOCVD reactors. For this study it was adapted to fit to FBH's Sentech SI500 ICP etch chamber that provides a glass window in the center of the top. The curvature measurement system (Fig. 2) consists of a light source unit that directs two parallel laser beams towards the wafer surface. If the wafer is bent, the distance between the reflected beams changes; this distance is evaluated by the system and allows the calculation of the bow.

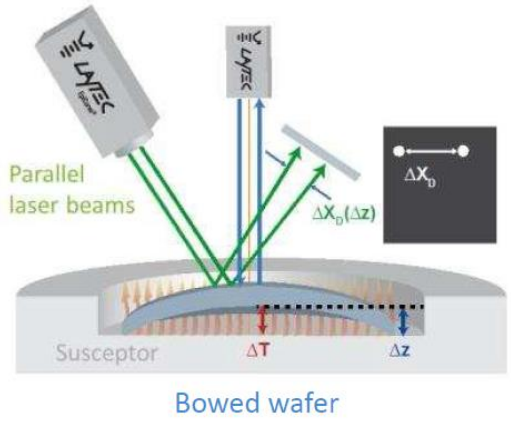

Fig. 2 Sketch of the wafer curvature measurement system

RESULTS

Fig. 3 shows as example the impact of the helium back cooling pressure on the bow of a 525 µm thick 100 mm SiC wafer bonded to a 105 mm diameter 1000 µm thick glass carrier. The bow increases linearly with increasing pressure up to 60 µm. Fig. 4 shows the course of the bow after optimization of the etch process parameters. The bow is now less than 40 µm during the whole process.

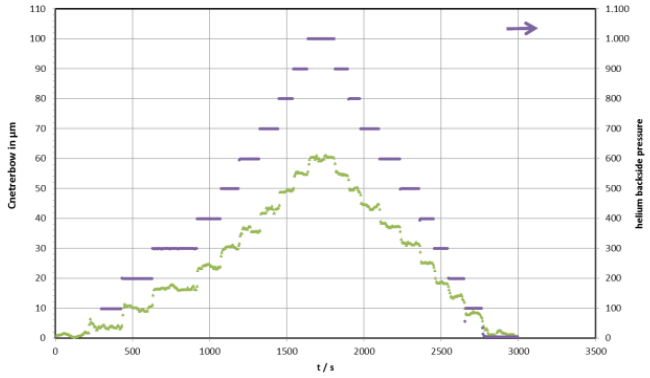

Fig.3 Impact of helium back pressure on bow of a 525 µm thick 100 mm SiC wafer bonded to a 1000 µm thick glass carrier.

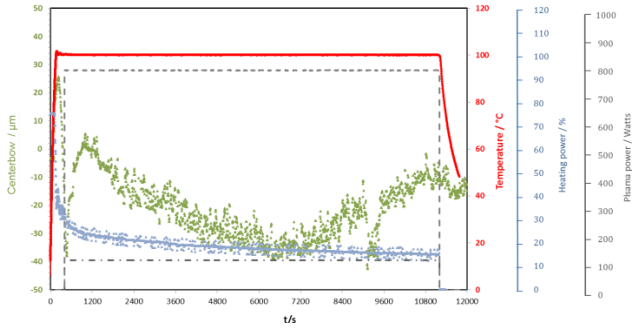

Fig.4 Wafer bow during the optimized SiC etch process of a 100 µm thick SiC wafer bonded to a 1000 µm thick glass carrier.

CONCLUSIONS

The application of the *in-situ* measurement system allowed the bow measurement of the wafer-carrier composite in the plasma etch chamber during etching. An independent determination of the contribution of the He back flow, the heating of the platen, the ICP and RF plasma power and the mechanical clamping on the wafer bow in the etch chamber was possible. This knowledge allowed to optimize the etch process by minimizing the stress on the thinned wafer, hence decreasing cracks and increasing the yield of the process.

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ACRONYMS

MMIC: monolithic microwave integrated circuits
ICP : inductively coupled plasma
TSV : through substrate vias
ITO : Indium tin oxide