Electrical Properties of GaN Etched by Low Bias Power Process

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Abstract

We have developed low damage GaN dry etching processes for recess gate GaN-HEMTs. In this study, the simple SBD structures, which were fabricated on GaN surface etched by ICP plasma, were used to evaluate the etching damage. In order to decrease the damage and inhibit degradation of Schottky barrier height (ϕb), extremely low bias power etchings were applied. As a result, since our BCl_3 etching processes under low bias power condition made the surface very rough, it was difficult to reduce the degradation of ϕb by etching. On the other hand, optimized Cl_2/BCl_3 etching process can realize smooth etched surface even if low bias power was used. Therefore, Cl_2/BCl_3 etching process achieved extremely low degradation of ϕb by etching.

INTRODUCTION

A millimeter-wave wireless network enables high-data rate communication without laying fiber optics. GaN high electron mobility transistors (GaN-HEMTs) have potential as devices for millimeter-wave amplifiers[1]. The operating speed can be improved by downscaling the gate-length. However, short gate-length HEMTs typically cause poor channel modulation. Therefore, the distance from the gate to the channel of HEMTs should be shortened to achieve excellent performance. Since thinning AlGaN layer leads to increasing sheet resistance, the use of gate recessing are expected for the short gate-length HEMTs.

Cl-based dry etching techniques are generally applied to fabrication process for recess gate GaN-HEMTs. However, during dry etching, the damage was often occurred due to generation of N or Ga vacancies, diffusion of impurities and generation of defects in crystal. This damage degrades the electrical properties of devices fabricated by using recess etching. This etching damage can be evaluated from some methods, such as Schottky properties[2,3]. However, there are few reports on Schottky properties of etched surface obtained from low bias power conditions.

In this study, we used simple SBD structures on etched GaN surface to evaluate the etching damage and tried to reduce the damage by using extremely low etching bias power.

EXPERIMENTAL

Si-doped n-GaN epitaxial structures were grown by MOCVD on sapphire substrates. Thickness of n-GaN and the doping concentration were designed to be 2 μm and 2×10^{17} cm^{-3}, respectively. n-GaN layers were etched by the inductively coupled plasma (ICP) dry etching system. The bias power was varied from 1.5 W to 20 W under BCl_3 or Cl_2/BCl_3 mixture condition. Etching time was adjusted so that etching depth became to be 100 nm. Surface morphologies of the etched n-GaN were observed by AFM. The 400 μm-diameter circular Ni/Au Schottky electrodes were fabricated on the etched surface. Capacitance-voltage (C-V) measurements of the Schottky electrodes were carried out to calculate ϕb.

RESULTS AND DISCUSSIONS

Figure 1 shows AFM images of GaN surface etched by our BCl_3 etching process. As shown in Fig.1(d), great smooth surface was obtained by using BCl_3 etching under 10 W bias power condition. However, low bias power etching tends to produce rough surface, such as Fig.1(b) and Fig.1(c). It is known that some solid state boron-chlorine compounds are generated in BCl_3 plasma. Then, these compounds deposit and inhibit etching[4]. The deposition might affect low bias power etching process with low etching rate and produce rough etching surface.

Figure 2 shows dependence of etching bias power of BCl_3 process on the normalized ϕb and RMS roughness. The normalized ϕb was calculated from ϕb (post etched samples)/ ϕb (as-grown sample). As shown in Fig.2, the normalized ϕb approached to 1 as decreasing bias power. This result insists that etching damage depends on bias power. However, even though their low bias power, the normalized ϕb of 1.5 W and 3 W were lower than that of 5 W. It was considered that rough etched surface strongly degrades ϕb. Therefore, both low bias power and smooth surface morphology were essential to realize low damage etching.

Figure 3 shows AFM images of GaN surface etched by optimized Cl_2/BCl_3 etching process. Figure 4 shows the bias power dependence on RMS roughness and comparison of BCl_3 etching process and Cl_2/BCl_3 etching process. These results show that Cl_2/BCl_3 etching can realize smooth etched surface even if it was low power condition, such as 2 W. It was considered that the amount of solid state compounds in Cl_2/BCl_3 mixture was lower than that of pure BCl_3, hence smooth surface can be realized under low bias condition.

As shown in Figure 5, low bias power Cl_2/BCl_3 etching processes achieved extremely low degradation of ϕb by etching. These results suggested that low bias power Cl_2/BCl_3 etching can be applied to low damage recess etching.

CONCLUSIONS

The authors reported on low damage etching of GaN using low bias power. The results of AFM measurements and C-V measurements of etched GaN surface showed that BCl_3 etching processes could not realize extremely low damage because of their rough surface. On the other hand, the optimized BCl_3/Cl_2 processes achieved great smooth surface and extremely low degradation of ϕb by low bias power etching, such as 2 W.

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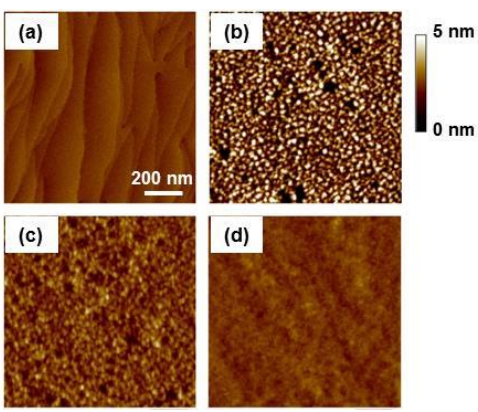

Fig. 1 AFM images of GaN surface etched by BCl_3 etching process ;(a)as-grown, (b)bias power 1.5 W, (c)bias power 3 W, (d)bias power 10 W.

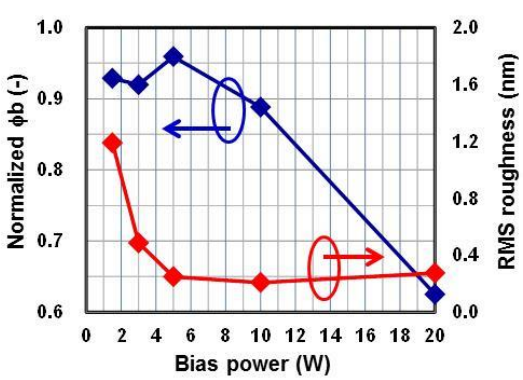

Fig. 2 Etching bias power dependence on the normalized ϕb and RMS roughness obtained from BCl_3 etching process.

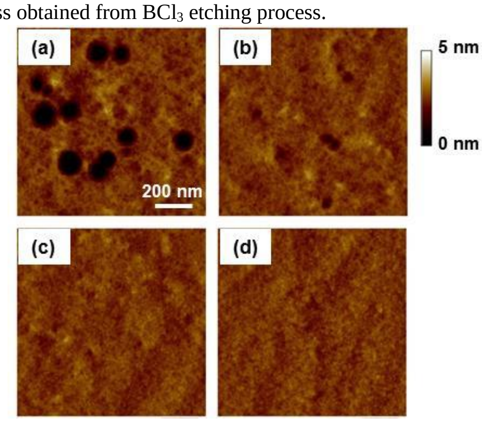

Fig. 3 AFM images of GaN surface etched by Cl_2/BCl_3 etching process ;(a)bias power 1.5 W, (b)bias power 2 W, (c)bias power 3 W, (d)bias power 10 W.

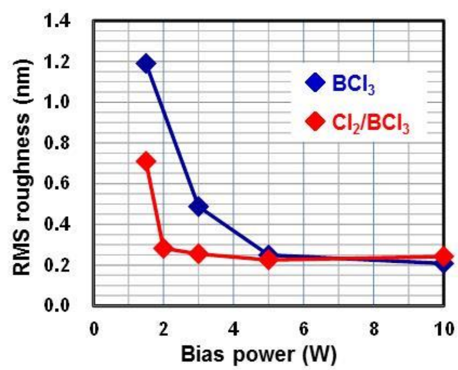

Fig. 4 Comparison of RMS roughness obtained from BCl_3 etching process and Cl_2/BCl_3 etching process.

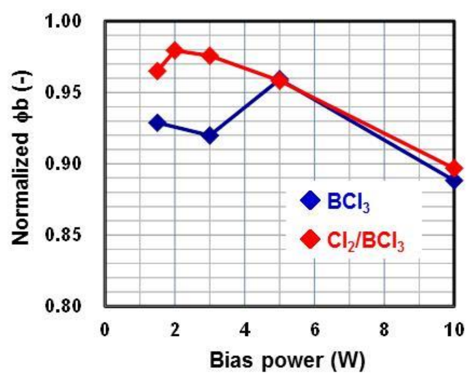

Fig. 5 Comparison of the normalized ϕb obtained from BCl_3 etching process and Cl_2/BCl_3 etching process.