

# ESD Protection Device for HEMT MMICs

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## Abstract

III-V high electron mobility transistors (HEMTs) have been widely used in Monolithic Microwave Integrated Circuits (MMICs) for power amplifiers, low noise amplifiers, and switches. More recently, Silicon on insulators (SOIs) and RF CMOS transistor have been used for the MMIC applications including those used in cellular PA modules. In comparison with the Si-based technologies, the lack of good electrostatic discharge (ESD) protection devices with a small footprint is one of the major drawbacks for HEMT MMICs.

In this study, two kinds of ESD protection devices are proposed for the HEMT MMICs. One approach is the multi-gate enhancement-mode HEMT power clamp, and the other is the optimized P-N junction diode. The multi-gate layout enables the small device footprint compared with the conventional power clamp scheme in which single gate devices are connected in series. Fig.1 illustrates the dual-gate FET layout. The gate is connected to the source/drain with a resistor. Since it can act as series connected diodes in the opposite direction, a large turn-on voltage of around 10 V is achieved in the both directions.

The gate multiplicity and the connection of gate resistors are chosen for each electrical terminal to be protected depending on the polarity and magnitude of the DC/RF voltages applied to the terminal during operation. Fig.2 shows two types of multi-gate FET layout with different gate resistor connections. The current turn-on characteristics are shown in Fig. 3. The HBM ESD protection capability can maintain the same level as Table.1 demonstrates.

The ESD protection capability is tested for two cases shown in Fig. 3. One is for the power clamp device alone, and the other is the power clamp device connected to a 0.02-pF MIM capacitor for protection. The schematic of the second case is attached in Fig. 4, and the result is shown in Table.2. HBM protection over 2kV is achieved for devices with the gate periphery 1000um or larger for the three types of multi-gate power clamps. For the case with the MIM capacitor, the power clamp device was damaged first.

The other approach is to utilize the P-N junction diode for ESD protection. Based on WIN semiconductors' BiHEMT technology which could integrate HBT and HEMT process in the same wafer, the base and collector layers can act as P-N junction diode. The HBM ESD protection level versus ESD protection device size is shown in Fig. 5. Over 2kV HBM ESD protection level is achieved with the  $484\mu\text{m}^2$  device size. In comparison with the multi-gate enhancement-mode HEMT power clamp, the device size is much smaller but the turn-on voltage is only 1.2V.

In conclusion, the new multi-gate enhancement-mode HEMT power clamp device provides over 2kV HBM ESD protection in HEMT MMICs with large and designable turn-on voltages in the both direction. The P-N junction diode can also provide the same HBM ESD level with smaller size and lower turn-on voltage. Choosing BiHEMT technology, circuit designers can select the suitable ESD protection device depends on the operating voltage. Combination of both approaches are expected to realize GaAs MMICs with high level ESD protection with minimal impact on the chip size and cost.

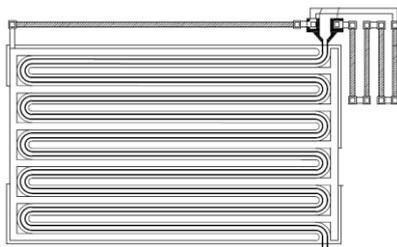


Fig 1A



Fig 1B

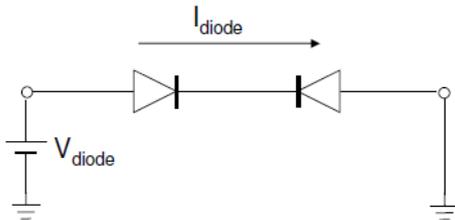


Fig 1C

Fig. 1 The A) layout, B) schematic, C) equivalent function block of the dual-gate HEMT power clamp

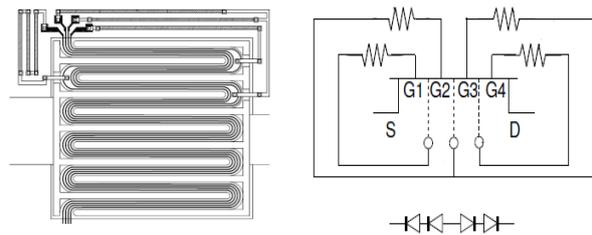


Fig 2B

Fig. 2 Examples of multi-gate clamp  
A) Triple gate HEMT power clamp,  
B) Quadruple gate HEMT power clamp

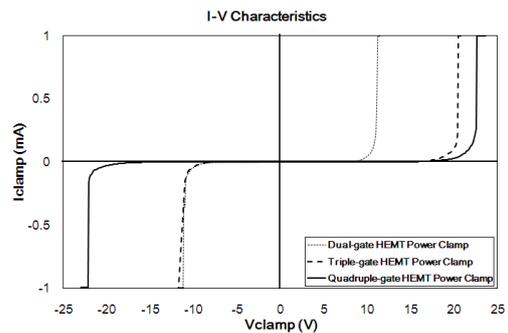


Fig. 3 I-V Characteristics of A)Triple  
B)Quadruple gate HEMT power clamp

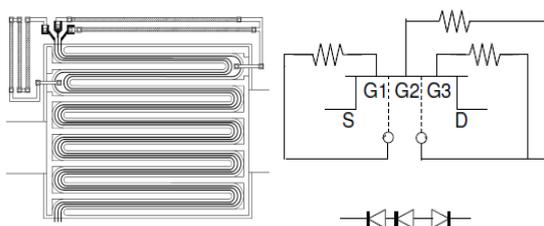


Fig 2A

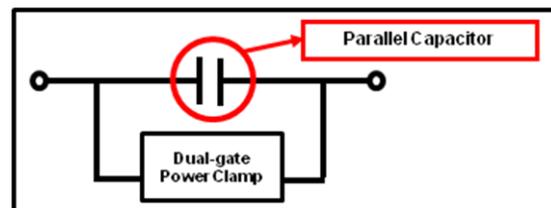
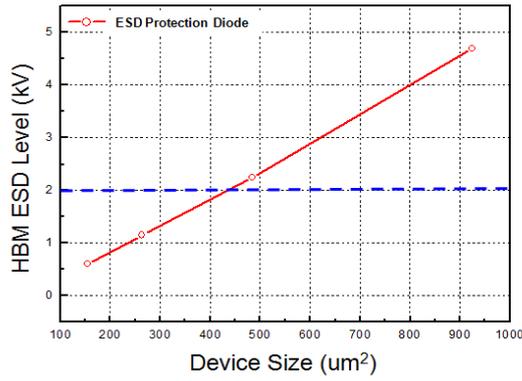


Fig. 4 Schematic of the capacitor which is parallel-connected to the dual-gate power clamp



**Fig.5 HBM ESD protection level versus ESD protection P-N diode size**

**Table. 1 HBM ESD protection level versus Device gate periphery**

Gate Periphery (um)	Dual-gate	Triple-gate	Quadruple-gate
HBM ESD Level (kV) (DUT : Multi-gate HEMT Clamp)	2.1	2	2

**Table. 2 HBM ESD protection level versus Device gate periphery**

Gate Periphery (um)	750	1000	1250	1500
HBM ESD Level (kV) (DUT : Dual-gate HEMT Clamp)	1.6	2.1	2.5	3.0
HBM ESD Level (kV) (DUT : Capacitor protected by dual-gate HEMT Clamp)	1.6	2.1	2.5	3.0