Rapid Production Readiness Through Process Margin Study: How to Isolate the Epi and Fab Parameters That Really Matter

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Introduction

The critical challenge during III-V device process development is to deliver a high performance technology rapidly and with high yield at process release. In 2014, Qorvo developed a new HBT technology for high performance power amplifiers for cellular and infrastructure applications. In the past, typical development timelines were two years from initiation to first ramp. By speeding up the development timeline to less than one year, development is being done with fewer wafer starts over a shorter period. The result is faster development but added risk for initial yield learning to overlap with initial production ramp. Process margin studies accelerated yield learning and revealed areas for focused process stability improvements to demonstrate a stable, high-yielding process. During development, resources for high volume manufacturing readiness can be hard to come by, but the results of the process margin study demonstrate that yield improvement before launch is time well-spent.

Purpose

This paper describes process margin study methodology as part of an overall program to deploy new epi and fab process flows. As part of developing a new HBT technology, the Qorvo development team:

(A) Identified test parameters dependent on process variables in fab and epi
(B) Ran experiments to gather sensitivity of parameter vs. process variables
(C) For parameters with high sensitivity to fab or epi, and whose variation is critical for either circuit performance or for yield, took action to reduce variation

A series of epi, fab, and epi/fab cross-term experiments were run through the fab on the new process flow. Emitter, base, collector and subcollector process variables were explored.

Emitter Layer-Base Contact Experiment

This paper will focus on the emitter and base cross-term experiment where base metal depth and emitter layer thickness were variables. The new base metal process is stable and does not induce variation in PCM data, but the emitter layer thickness is critical for especially Cbe, Bvebo and surface leakage between emitter and base contacts.

The new HBT process uses an InGaP emitter layer with a base metal contact that is alloyed into the base layer. To characterize the process corners, the experiment included deep base metal with thin InGaP and shallow base metal with thick InGaP. Adding the center condition for base metallization while varying just the InGaP thickness provided a separate sensitivity value for epi and base metal variables.

		Fab: Base metal depth		
		-23%	POR	+23%
Epi: InGaP emitter layer thickness	-10%	X	X	X
	POR		X	
	+10%	X	X	X

Figure 1: Emitter layer thickness and base metal depth variants and cross-terms

Emitter-base sidewall leakage dependence on emitter layer thickness is shown in Figure 2. Base metal depth has no impact, on leakage, but emitter layer thickness variation of +/-20% changes leakage by more than one order of magnitude. Likewise, for Bvebo and Cbe, base metal depth had no impact on parametric variation, but epi layer thickness had a strong impact.

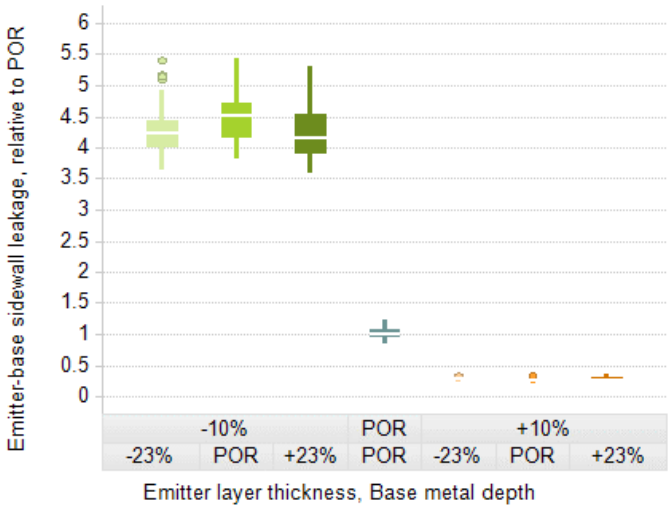

Figure 2: Emitter-base leakage for each emitter layer and base metal depth combination.

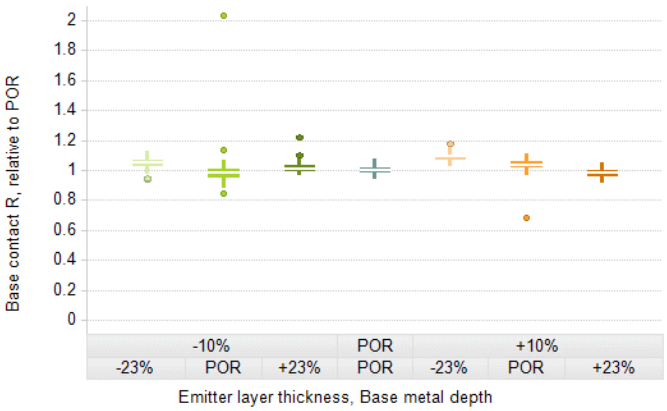

Figure 3: Base contact resistance for each emitter layer thickness and base metal depth combination.

After demonstrating that a strong process-parametric relationship existed, the next step toward production readiness was to take action on the information. Among the process margin study variants, those with little parametric impact were eliminated from further study. As shown in Figures 2 and 3, base metal depth was one such process variable, as it had no measurable impact on emitter-base leakage (Fig. 2) or on base contact resistance (Fig. 3), base transfer length, Vbc or Cbc (not shown here). Of the remaining process variables, further study was done only on those shown to have both a significant correlation to the PCM parameter and account for more than 20% of the overall process variation observed to date. In the cases of Cbe, Bvebo and base-emitter leakage, each parameter had ≥ 50% of its variation attributed to emitter layer thickness variation, so the correlations are especially strong.

Actions to Assure High Initial Yields

For process steps with strong interactions, those parameters with the most impact on circuit designers were considered first. Foremost among the DC parameters are Beta and Cbc, with emitter, base and collector resistances following. Primary impacts are all in the epi layers: layer thickness, doping and composition require tight control. The steps taken to assure high initial yield will be discussed, and include:

1. Share results from epi/fab process margin studies internally and with the supplier
2. Understand the control plan, especially for processes affecting RF parameters that can't easily be prescreened during the fab and PCM process. Where possible, tighten controls on the process.
3. Improve screening methods and tighten specification limits as needed. This step implies Cpk reduction and should be avoided if possible.

For next-generation HBTs, only steps 1 and 2 were required. We will discuss three process margin studies and the resulting actions leading to high initial yields.